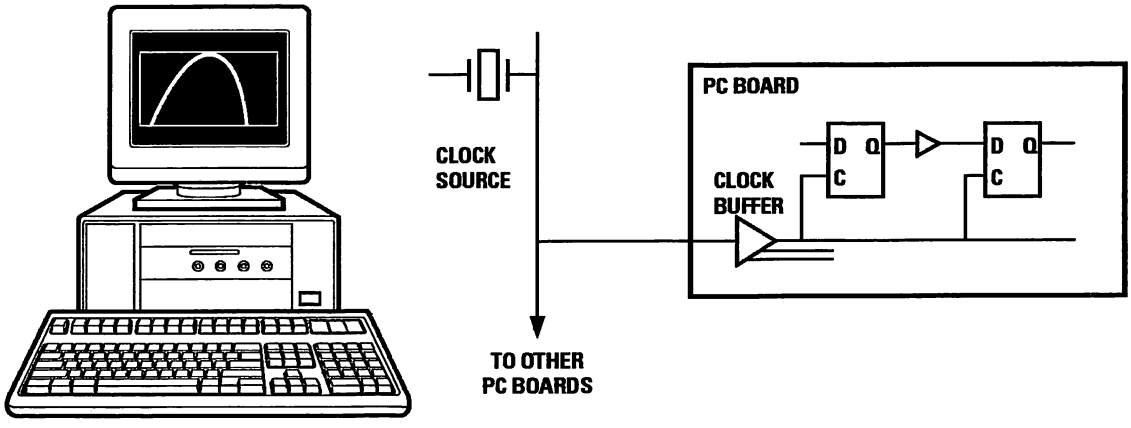
HEWLETT® PACKARD

Characterize and Reduce Clock Jitter to Improve System Speed and Reliability

HP E1725A Option 243 Time Interval Analyzer

HP E1743A Clock Jitter Analyzer Software

HP E1740A Time Interval Analyzer Module



The HP E1743A Clock Jitter Analyzer Software provides digital designers with a powerful tool for understanding and reducing jitter in clock distribution networks and buffers.

Jitter plagues designers of high speed clock distribution networks found in such diverse digital products as microprocessors, PCs, computer mainframes, workstations, super computers and instruments. Jitter is also a concern for designers of the clock buffers found in these networks such as PLLs, frequency dividers, fanout and translation ICs. As clock speeds increase, jitter can consume a significant portion of the timing budget and cause errors (or metastable conditions).

By reducing jitter, you can reduce the errors or increase the clock speed, thereby improving your system performance. The HP E1743A software helps you reduce jitter by accurately characterizing its extent and identifying its cause.

The HP E1743A software integrates measurement functions of the HP E1740A Time Interval Analyzer (TIA) module with powerful Microsoft® Windows-based analysis routines that run on an IBM-compatible PC. The HP E1725A TIA with Option 243 combines both the software and TIA module into a complete instrument with everything you need to make clock jitter measurements. You can also purchase individual components for integration into your own system.

The HP E1725A Option 243 TIA displays jitter in the modulation domain with "vs. time" displays (measurements as a function of time). These displays show phenomena like cycle-to-cycle variation and long term drift. When characterizing a PLL, the vs. time display also simplifies analysis of lock times, phase step recovery, and phase delay from input to output. Time and phase deviation displays compare edge placement of a measured clock with an ideal clock. The FFT of a vs. time display reveals periodic components of jitter and helps identify its source. Histograms are another way to characterize jitter, providing statistics such as rms and peak-to-peak jitter.

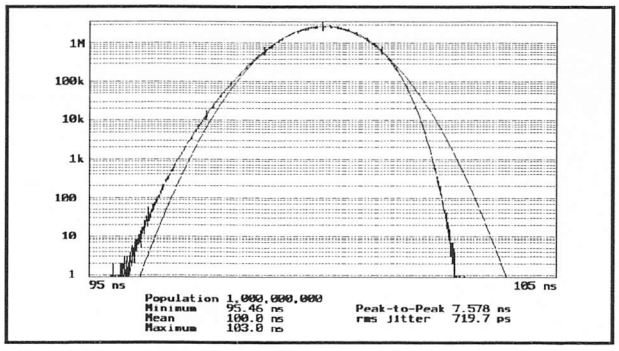
Powerful Ways to Measure and Display Jitter Give Confidence in Results

Peak-to-Peak and Cycle-to-Cycle Jitter

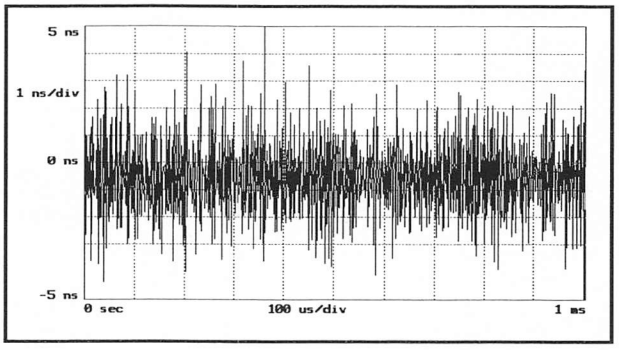
By definition, jitter is measured by comparing the placement in time of one edge to other similar edges. To measure peak-to-peak jitter, you must capture many edges. For example, a computer clock distribution system design may need to guarantee a confidence level of 1 error in 1 billion clock cycles (with a 50 MHz clock, this means 1 error every 20 seconds). To measure cycle-to-cycle jitter, you must capture every edge. You don't want to miss those rare short and long cycles that cause errors.

The HP E1725A Option 243 TIA captures every clock cycle up to 80 MHz, continuously, for a trillion cycles using fast histogram, or 32k cycles using a vs. time display. You get complete statistics, including the peaks (pk-pk, +pk, -pk), mean and standard deviation (rms jitter). Now you can get the true accumulated peak-to-peak jitter value, not just an estimate. You can also get the maximum and minimum displacements from the cycle-to-cycle display.

Fast data acquisition is also important in jitter measurements so that long-term drift doesn't mask the true peak-to-peak value. For example, suppose you have a 50 MHz clock and want to measure the peak-to-peak jitter of 1 billion clock cycles. Because the HP E1725A Option 243 TIA captures every cycle, it will take only 20 seconds to acquire 1 billion clock cycles—not much time for long-term drift to affect the results.



Distribution of 1 billion clock cycles shows the true peak-peak, min, max and rms jitter. Comparison to a normal distribution shows that the jitter is not being caused by random noise.



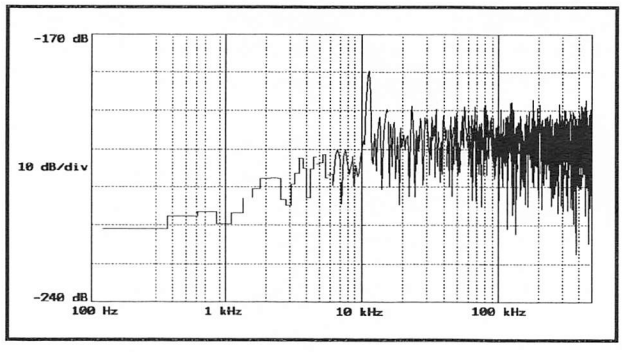
This cycle-to-cycle display shows rare short clock cycles that can cause errors.

Determining the Source of Jitter Leads to Better Performance

To improve your system performance, the HP E1725A Option 243 TIA has a built-in FFT to display the spectral components of jitter (Jitter Spectrum). This helps you determine the jitter's root cause and eliminate it. For example, assume you are using a PLL as your clock distribution device, and a histogram of 100 million clock cycles shows that the distribution is not Gaussian.

The FFT of the vs. time display might reveal a periodic jitter component of 50 or 60 Hz or some multiple thereof. You then know you need to better isolate the PLL from the AC line frequency. Once you do that, the histogram shows less jitter and your system will exhibit fewer errors. Or, you could decide to increase the clock speed and, therefore, your system performance.

Analyze networks for unwanted jitter. The FFT quickly points out a jitter component at approximately 11 KHz. Eliminate it to reduce jitter and increase production timing margin.



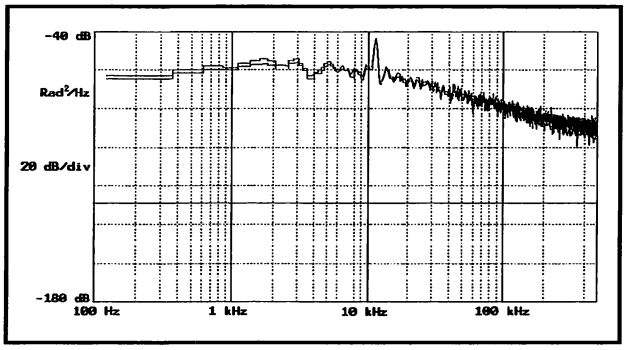
Flexible Ways to Analyze Jitter

Since there are no industry-wide standards for measuring clock jitter, the HP E1725A Option 243 TIA offers a variety of methods. You've already seen the power of cycle-to-cycle displays, histograms and FFTs.

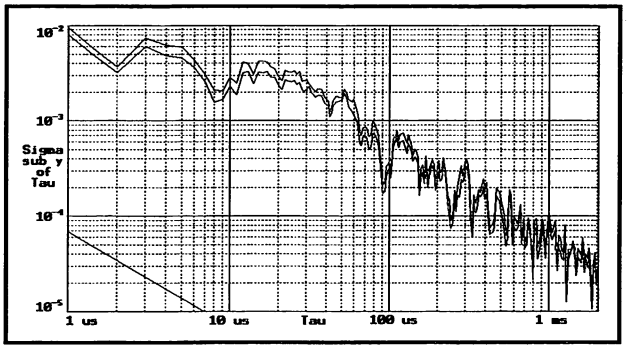
However, you may be more familiar with thinking about jitter as phase noise in the frequency domain. You'll want the Power Spectral Density display which shows phase noise as noise power offset from the carrier.

Or, you may be working with a crystal oscillator or other clock source, and are more familiar with thinking about jitter as frequency stability (noise and drift). Then you'll want the Allan Variance display which plots $\sigma_y(\tau)$ as a function of time. This gives you knowledge of the type and level of noise (white phase, flicker phase, random walk phase, flicker FM, random walk FM, and white FM).

No matter which way you choose to look at jitter, the software is written in your language. You decide how you want the data to be displayed.



Find the amount of noise power in a given bandwidth with the power spectral density display.

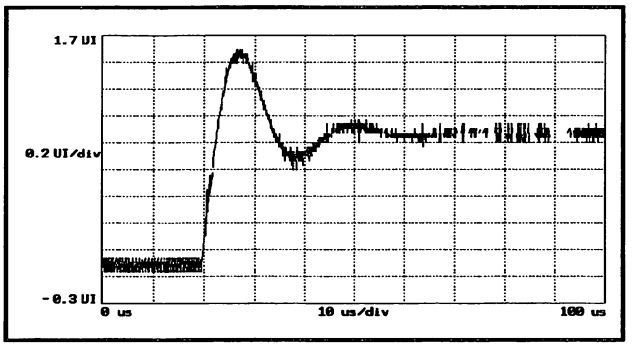


The Allan Variance display helps you characterize oscillator stability.

Other Related Clock Timing Measurements Speed Analysis of System Dynamics

If you manufacture clock distribution ICs, such as PLL parts, you may need to measure the sensitivity of your part to dynamic power supply variations. For example, how much does the clock phase shift when supply voltages change during a RAM write cycle, and how long does it take to recover? The time and phase deviation displays of the HP E1725A Option 243 TIA quickly reveal this.

You might also want to know how long it takes your part to lock onto the clock's phase/frequency when first turning on the system. Or you may need to know the phase relationship between the input and output of the PLL to make sure that there is no net phase delay through the part. Use the vs. time display to measure these.



The output of this PLL took about 40 µs to readjust after a one cycle long drop-out of the clock input.

Export Data and Graphics to External Programs for Additional Analysis

When you need superior analysis flexibility, you can export data in a variety of formats. This allows for analysis in a wide variety of other software, either off-the-shelf or custom designed.

For example, you can use the Windows Clipboard to copy data to other Windows applications, such as Microsoft Excel or Lotus® 1-2-3®. Or store data in ASCII text files for use by applications that support this format, such as MathCad. You can copy the instrument's display to the clipboard, so you can paste it into a report prepared with a Windows word processor such as Microsoft Word, or Lotus Ami Pro.

Flexible Configuration Meets Your Needs

Choose either a complete instrument or configure your own VXI-based measurement system.

For a complete instrument, simply order the HP E1725A with Option 243—this combination comes with everything you need to make clock jitter measurements. Just connect the accessories, turn on the power, and you're ready to start making measurements.

Five HP E1725A options cover your customization needs when you need something a little different from the standard instrument configuration. Three of these options add additional capabilities to the embedded computer: 16 MB memory, GP-IB interface, and software to allow custom control of any VXI module. Another option deletes the embedded computer and adds an HP-IB interface—you add your own PC with an HP-IB module. If you want to add more than one VXI module, another option replaces the 5-slot mainframe with a 13-slot one.

When you need complete flexibility, just order the separate pieces—HP E1740A Time Interval Analyzer VXI module, HP E1743A Clock Jitter Analysis Software, VXI mainframe, computer, Slot-0 controller, and other VXI modules.

See the separate Configuration Guide for complete information.

Key Specifications

HP E1743A Clock Jitter Analyzer Software

Measurements

- **Vs. time:** Period, Frequency, Time Interval, Phase, Cycle-to-Cycle
- **Deviation:** Period, Frequency, Time Interval, Phase
- **FFT:** Of any vs. time or deviation display; power spectral density
- **Histogram:** Of any vs. time or deviation display; fast histogram
- **Frequency Stability:** Allan Variance
- **Statistics:** Minimum, maximum, peak-to-peak (range), mean, rms (standard deviation)

Continuous sequential memory: 32k cycles
Continuous histogram memory: 1 trillion cycles

HP E1740A Time Interval Analyzer Module

Maximum clock frequency: 150 MHz
Maximum cycle-to-cycle frequency: 80 MHz
Analog input bandwidth: 200 MHz
Measurements: Time Interval: 1→1, 1→2, 2→2
Resolution: 50 ps LSD; <100 ps rms
Maximum measurement memory: 512k samples

For more information:
HP E1743A/E1740A/E1725A
Price List, pub. no. 5962-7254E/EUS.
HP E1743A/E1740A/E1725A
Technical Specifications,
pub. no. 5962-7253E.
HP E1743A/E1740A/E1725A
Configuration Guide, pub. no.
5962-7255E.

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