Passively Probing a Motorola MPC 860/821 BGA Target System with Agilent Technologies E5346A High-Density Termination Adapters

Product Note
Solutions for Digital System Debug

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Passively Probing a Motorola MPC 860/821 BGA Target System with Agilent Technologies E5346A High-Density Termination Adapters

This product note describes how to connect a Agilent Technologies logic analyzer to the BGA package of a Motorola MPC 860/821 target system for use with an inverse assembler.

Signals required for inverse assembly are shown in the pinout information beginning on page 7 and must be routed to AMP Mictor 38 connectors for connection to the logic analyzer.

Six, 16-channel logic analyzer pods are required for inverse assembly.These six pods are connected via the Mictor connectors to three E5346A high-density termination adapters. The termination adapters are not included with the inverse assembler and must be ordered separately.

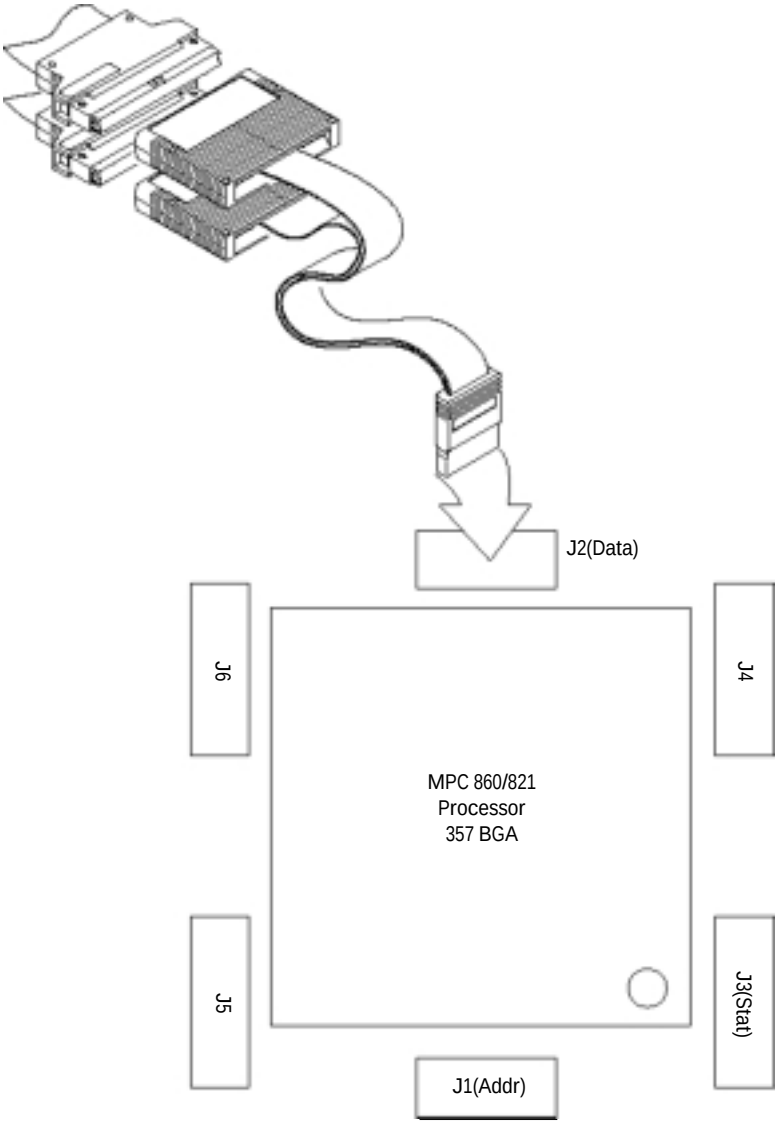

Figure 1. Connector Layout for the MPC 860/821 BGA Target

Direct Connection through E5346A High-Density Adapter Cables

The E5346A high-density adapters use a minimal amount of board space. Each high-density adapter connects to two logic analyzer pods, providing 32 channels of logic analysis per connector and access to two clock pins, as shown in figure 2.

Grounds need to be connected to pin 3 of the AMP Mictor connector. SCL, +5VDC and SDA are not to be connected to the target system (pins 1, 2, and 4 on the Mictor connector).

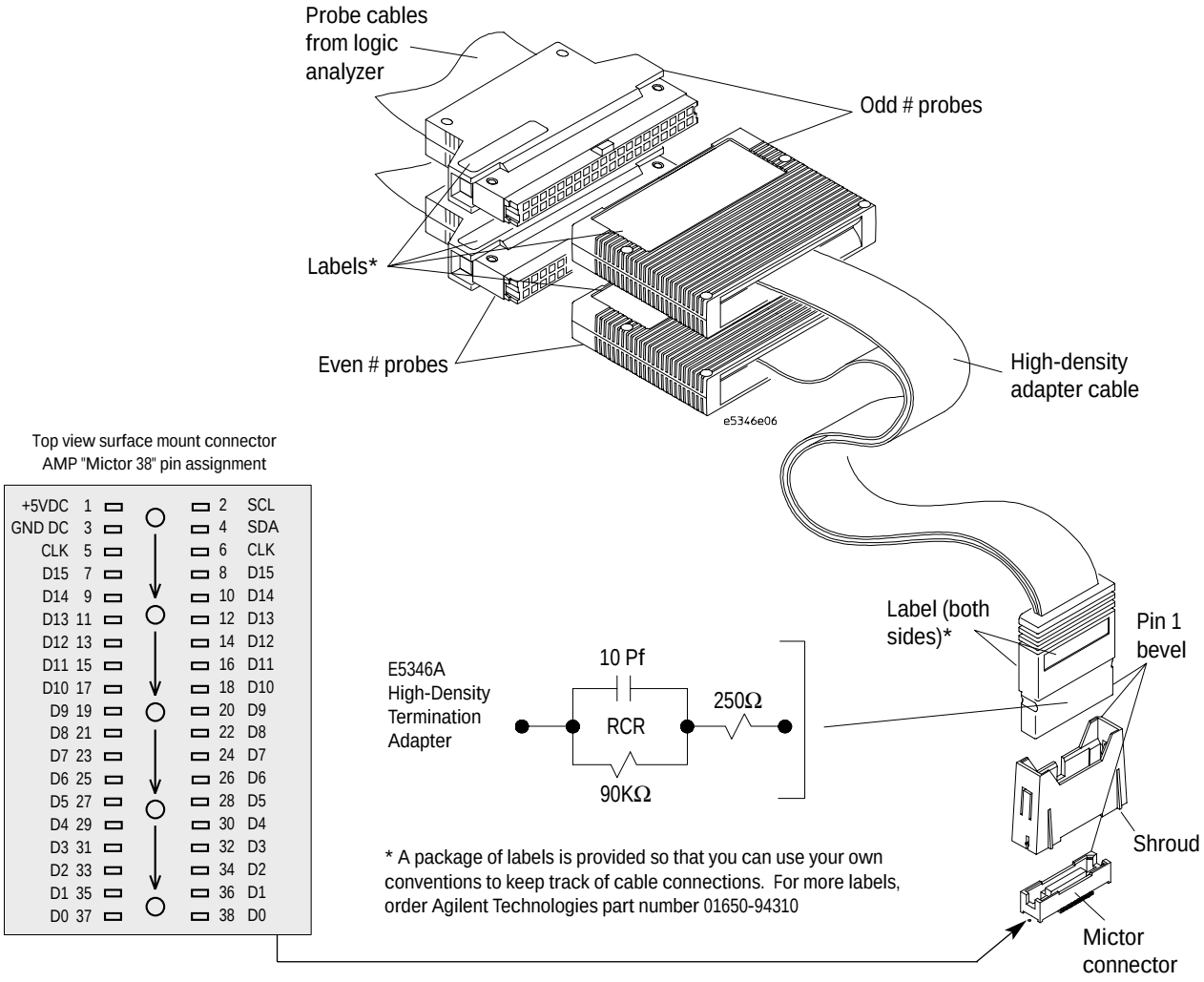

Figure 2. E5346A High-Density Termination Adapter

Termination for logic analysis is included at the probe tip of the E5346A high-density termination adapter for easy application and use. A schematic of this termination is shown in figure 3.

The AMP Mictor connector must be placed close enough to the target system so that the stub length created is less than 1/5 the Tr (bus risetime). For PC board material (er=4.9) and Zo in the range of 50-80Ω , use a propagation delay of 160 ps/inch of stub.

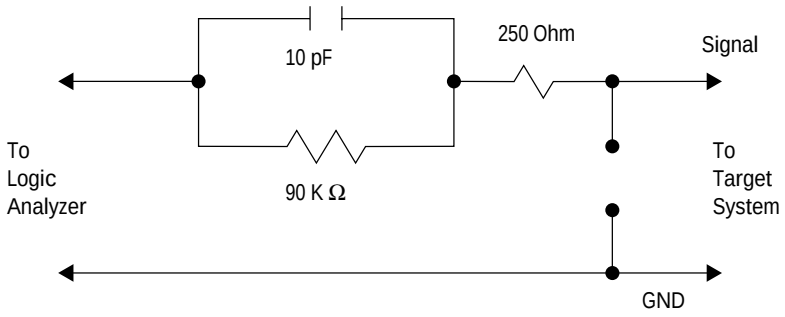

Figure 3. RC Network for Signal Termination

Three E5346A adapters and Mictor connectors are needed to probe all the required signals for inverse assembly.

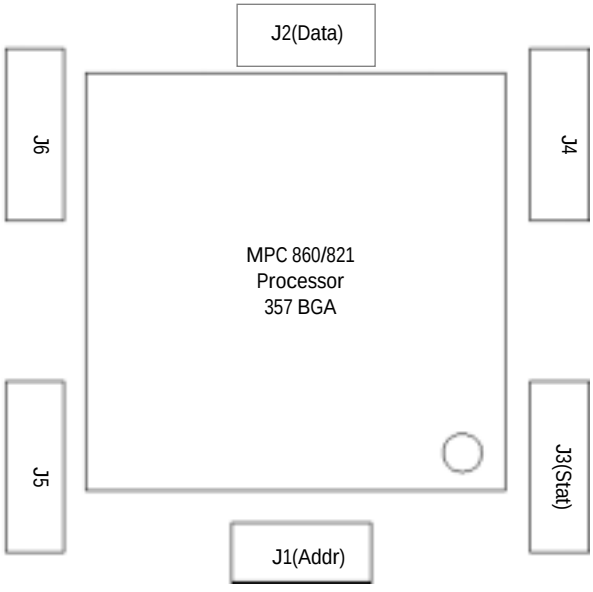

Figure 4. Mictor Connector Placement

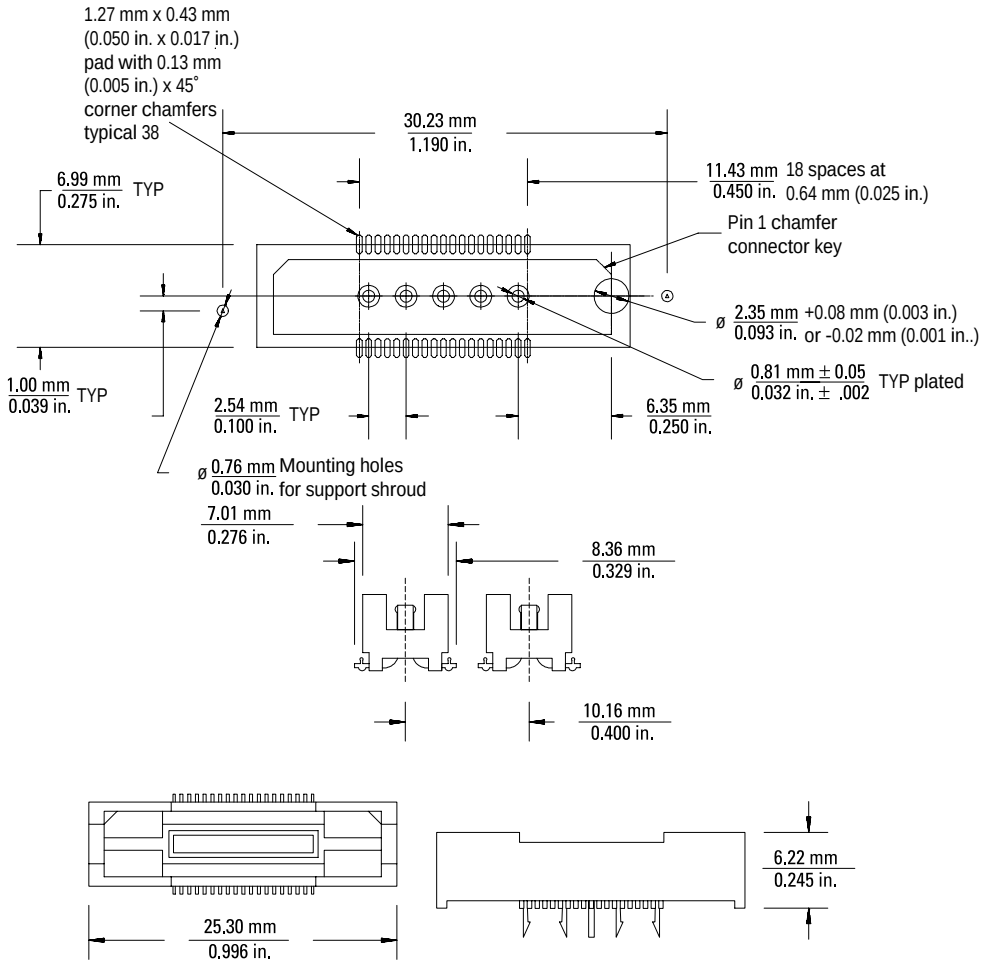

Figure 5. AMP Mictor Connector Dimensions

Mictor Connector Placement

Placing the AMP Mictor connectors as close as possible to the signal source will minimize stub length and ensure a reliable measurement. Figure 4 shows the connector layout of J1-J6. J1-J3 are required for inverse assembly. J4-J6 are optional for timing and state analysis of I/O ports.

Mictor Connector

The AMP Mictor connectors are available from AMP (PN 2-767004-2) or from Agilent (PN E5346-68701). The Agilent Mictor kit contains five AMP Mictor connectors and five support shrouds. The signals +5 V DC, SCL, and SDA are not used for probing and should not be connected to the target system, as shown in figure 2.

Support Shroud

A support shroud (Agilent E5346-44701) is recommended to provide additional strain relief between the Agilent E5346A adapter and the AMP Mictor connector, as shown in figure 5. The shroud fits around the AMP Mictor connector and requires two through-hole connections to the target board. Five shrouds are included with five AMP Mictor connectors in the E5346-68701 kit.

Inverse Assembler

An inverse assembler translates logic levels captured by the logic analyzer into MPC 860/821 mnemonics and identifies the microprocessor bus cycles captured, such as memory read/write, interrupt acknowledge, or I/O read/write.

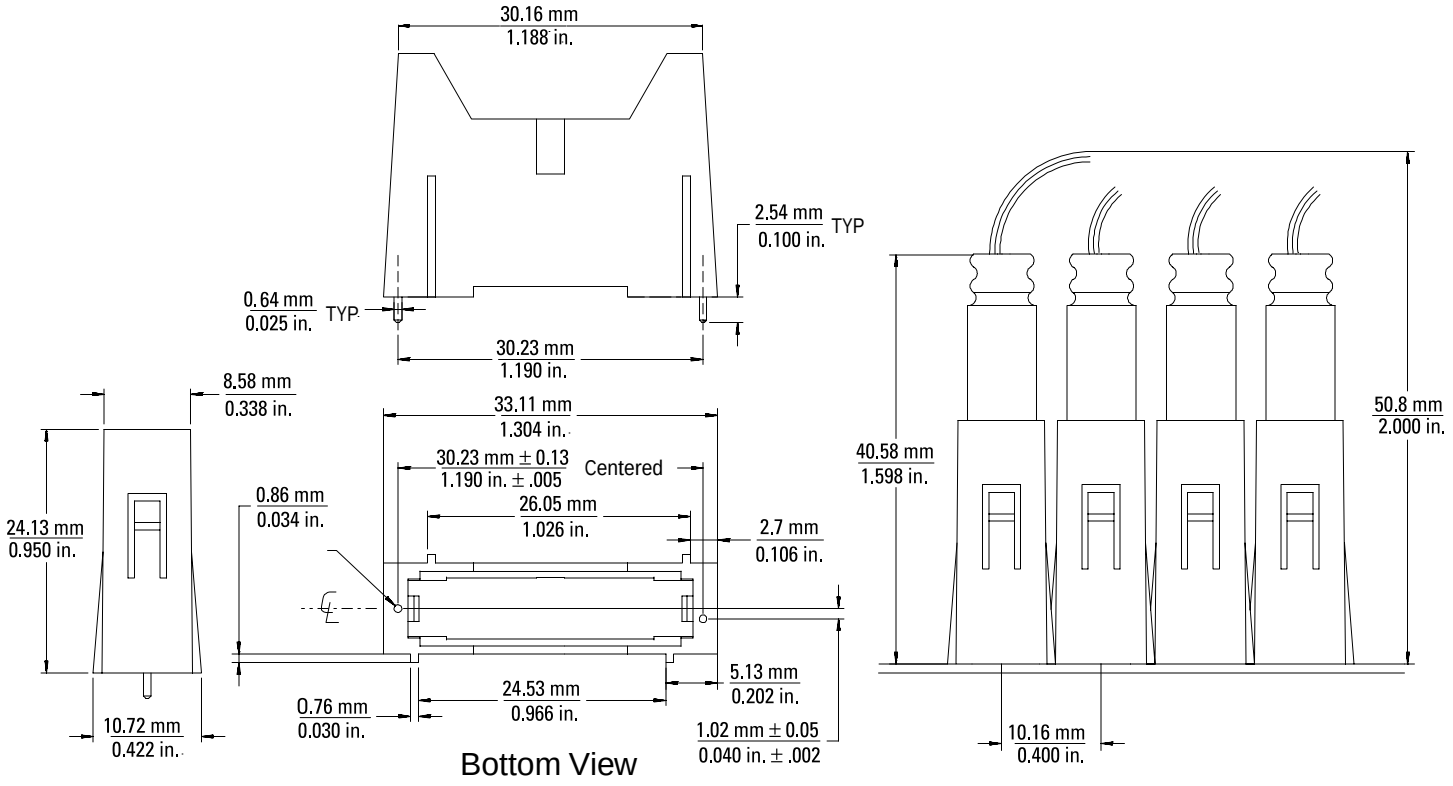

Figure 6. Support Shroud Dimensions

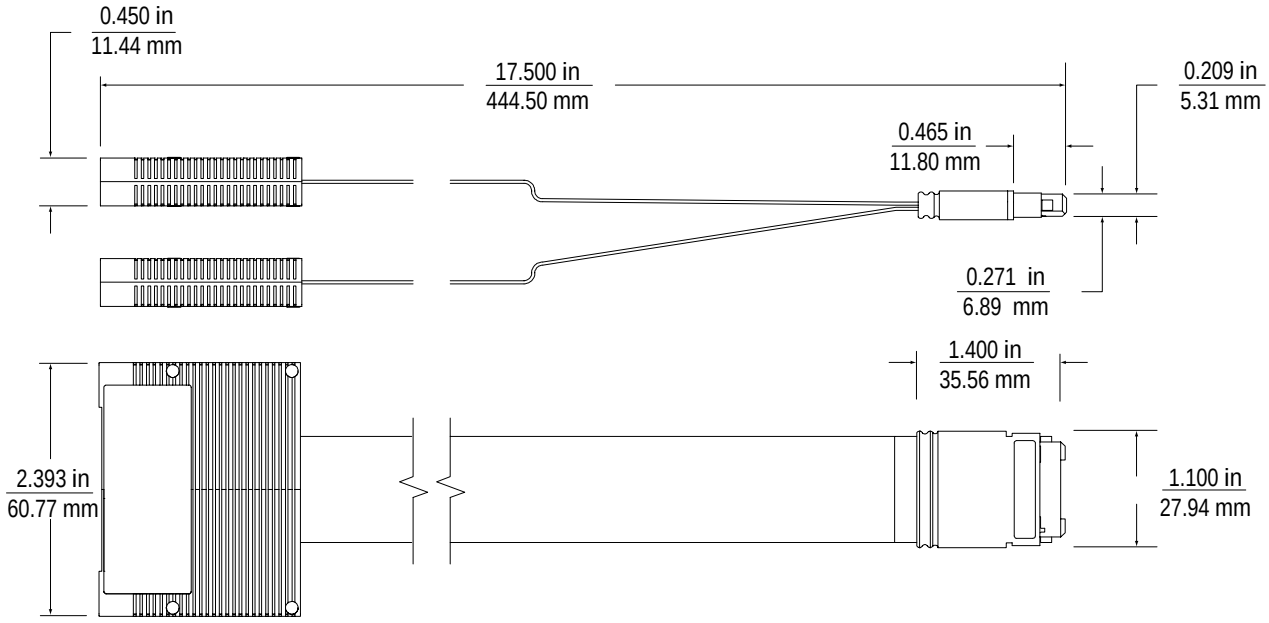

Figure 7. High-Density Termination Adapter Cable Dimensions

Source Correlation Tool Set

The inverse assembler can be used with the B4620B source correlation tool set. This allows you to time-correlate an acquired trace to written code. The source correlation tool set uses the information provided in your object file to build a database of source files, line numbers and symbol information.

IEEE 695, Elf/Dwarf, and ASCII symbol files are supported.

Pin-Out Information on Required Signals for Inverse Assembly

This table describes the three Mictor 38 connectors necessary for compatibility with the inverse assembler and the E5346A high-density termination adapter cables. This is intended to be a guide for placing probing connectors on a target system.

For the inverse assembler, the J1, J2, and J3 connectors listed below must be connected through the three high-density adapter cables. For simultaneous timing and state analysis for all signals, additional connectors must be used.

Note: * - Active Low

Mictor 38		Logic Analyzer		Microprocessor	
Conn.	Pin#	Pod #	Bit#	Pin#	Signal name
J1	38	1	0	A9	A31(LSB)
	36		1	A11	A30
	34		2	A12	A29
	32		3	A10	A28
	30		4	A13	A27
	28		5	C10	A26
	26		6	D10	A25
	24		7	C11	A24
	22		8	B11	A23
	20		9	B10	A22
	18		10	B12	A21
	16		11	C12	A20
	14		12	D11	A19
	12		13	D9	A18
	10		14	B13	A17
	8		15	C13	A16
	6		CLK	L1	*STS
J1	37	2	0	D12	A15
	35		1	A14	A14
	33		2	B14	A13
	31		3	C14	A12
	29		4	A15	A11
	27		5	B15	A10
	25		6	C15	A9
	23		7	D15	A8
	21		8	A16	A7
	19		9	B16	A6
	17		10	A17	A5
	15		11	B17	A4
	13		12	C16	A3
	11		13	A18	A2
	9		14	B18	A1
	7		15	B19	A0(MSB)
	5		CLK	W3	CLKOUT*

Mictor 38		Logic Analyzer		Microprocessor	
Conn.	**Pin#**	**Pod #**	**Bit#**	**Pin#**	**Signal name**
J2	38	3	0	T7	D31(LSB)
	36		1	U6	D30
	34		2	W5	D29
	32		3	V6	D28
	30		4	V12	D27
	28		5	U7	D26
	26		6	T8	D25
	24		7	V7	D24
	22		8	U12	D23
	20		9	T9	D22
	18		10	U8	D21
	16		11	V8	D20
	14		12	U9	D19
	12		13	V9	D18
	10		14	T12	D17
	8		15	U10	D16
	6		CLK	C9	TS1Z1
J2	37	4	0	T10	D15
	35		1	V10	D14
	33		2	V13	D13
	31		3	T13	D12
	29		4	U11	D11
	27		5	V11	D10
	25		6	T11	D9
	23		7	U13	D8
	21		8	W6	D7
	19		9	W7	D6
	17		10	W9	D5
	15		11	W13	D4
	13		12	W10	D3
	11		13	W11	D2
	9		14	W12	D1
	7		15	W14	DO (MSB)
	5		CLK	B9	TS1Z0
J3	38	5	0	A5	WE3*/BS_B3*/PCWE*
	36		1	B6	WE2*/BS_B2*/PCOE*
	34		2	A6	WE1*/BS_B1*/IOWR*
	32		3	C7	WE0*/BS_B0*/IORD*
	30		4	B8	BS_A3*
	28		5	A7	BS_A2*
	26		6	C8	BS_A1*
	24		7	D8	BS_A0*
	22		8	C4	CS7*/L_CE2_B*
	20		9	D5	CS6*/L_CE1_B*
	18		10	B4	CS5*
	16		11	A4	CS4*
	14		12	E4	CS3*
	12		13	D4	CS2*
	10		14	A2	CS1*
	8		15	C3	CS0*
	6		CLK	D1	TEA*

Mictor 38		Logic Analyzer		Microprocessor	
Conn.	**Pin#**	**Pod #**	**Bit#**	**Pin#**	**Signal name**
J3	37	6	0	F3	TS*
	35		1	B2	RD/WR*
	33		2	F1	BURST*
	31		3	D2	BDIP/GPLB5*
	29		4	E3	BI*
	27		5	G4	BR*
	25		6	E1	BB*
	23		7	E2	BG*
	21		8	H1	IP_B7/PTR/AT3
	19		9	K3	IP_B6/DSDI/AT0
	17		10	J4	IP_B5/LWP1/VF1
	15		11	G2	IP_B4/LWP0/VF0
	13		12	G1	IP_B3/LWP2/VF2
	11		13	J2	IP_B2/IOIS16_B*/AT2
	9		14	J3	VFLS1/IP_B1/IWP1
	7		15	H2	VFLS0/IP_B0/IWP0
	5		CLK	C2	TA*
J4	38	7	0	T3	IP_A7
	36		1	T6	IP_A6
	34		2	U5	IP_A5
	32		3	U4	IP_A4
	30		4	W2	IP_A3
	28		5	U3	IP_A2/IOIS16_A*
	26		6	T4	IP_A1
	24		7	T5	IP_A0
	22		8	K1	KR*/IRQ4*/SPKROUT
	20		9	G3	FRZ/IRQ6*
	18		10	V4	DP3/IRQ6*
	16		11	W4	DP2/IRQ5*
	14		12	V5	DP1/IRQ4*
	12		13	V3	DP0/IRQ3*
	10		14	F2	CR*/IRQ3*
	8		15	H3	RSV*/IRQ2*
	6		CLK	K2	ALEA
J4	37	8	0	B3	CE1_A*
	35		1	B1	UPWAITB*/GPLB4*
	33		2	C1	UPWAITA*/GPLA4*
	31		3	R3	WAIT_A*
	29		4	R4	WAIT_B*
	27		5	P2	SRESET*
	25		6	N4	HRESET*
	23		7	P3	RSTCONF*
	21		8	R2	PORESET*
	19		9	M4	OP3/MODCK2/DSDO
	17		10	L1	OP2/MODCK1/STS*
	15		11	L2	OP1
	13		12	L4	OP0
	11		13	N3	TEXP
	9		14	J1	ALEB/DSCK/AT1
	7		15		
	5		CLK	N2	EXTCLK

Mictor 38		Logic Analyzer		Microprocessor	
Conn.	**Pin#**	**Pod #**	**Bit#**	**Pin#**	**Signal name**
J5	38	9	0	C18	PA15/RXD1
	36		1	D17	PA14/TXD1
	34		2	E17	PA13/RXD2
	32		3	F17	PA12/TXD2
	30		4	G16	PA11/L1TXDB
	28		5	J17	PA10/L1RXDB
	26		6	K18	PA9/L1TXDA
	24		7	L17	PA8/L1RXDA
	22		8	M19	PA7/CLK1/TIN1/L1RCLKA/BRGOUT1
	20		9	M17	PA6/CLK2/TOUT1*/BRGCLK1
	18		10	N18	PA5/CLK3/TIN2/L1TCLKA/BRGOUT2
	16		11	P19	PA4/CLK4/TOUT2*
	14		12	P17	PA3/CLK5/TIN3/BRGOUT3
	12		13	R18	PA2/CLK6/TOUT3*/L1RCLKB/BRGCLK2
	10		14	T19	PA1CLK7/TIN4/BRGOUT4
	8		15	U19	PA0/CLK8/TOUT4*/L1TCLKB
	6		CLK	A3	CE2_A*
J5	37	10	0	D16	PC15/DREQ1*/RTS1/L1ST1
	35		1	D18	PC14/DREQ2*/RTS2*/L1ST2
	33		2	E18	PC13/L1RQB/ L1ST3
	31		3	F18	PC12/L1RQA/ L1ST4
	29		4	J19	PC11/CTS1*
	27		5	K19	PC10/CD1*/TGATE1*
	25		6	L18	PC9/CTS2*
	23		7	M18	PC8/CD2*/TGATE2*
	21		8	M16	PC7/L1TSYNCB/SDACK2*/CTS3*
	19		9	R19	PC6/L1RSYNCB/CD3*
	17		10	T18	PC5/L1TSYNCA/SDACK1*/CTS4*
	15		11	T17	PC4/L1RSYNCA/CD4*
	13		12	C6	OE*/GPLA1*/GPLB1*
	11		13	B5	GPLA2*/GPLB2*/CS2*
	9		14	C5	GPLA3*/GPLB3*/CS3*
	7		15	D3	GPLA5*
	5		CLK	D7	GPLA0*/GPLB0*
J6	38	11	0	C17	PB31/SPISEL*/RRJECT1*
	36		1	C19	PB30/SPICLK
	34		2	E16	PB29/SPIMOSI
	32		3	D19	PB28/SPIMISO/BRGOUT4
	30		4	E19	PB27/I2CSDA/BRGOUT1
	28		5	F19	PB26/I2CSCL/BRGOUT2
	26		6	J16	PB25/SMTXD1
	24		7	J18	PB24/SMRXD1
	22		8	K17	PB23/SMSYN1*/SDACK1*
	20		9	L19	PB22/SMSYN2*/SDACK2*
	18		10	K16	PB21/SMTXD2/L1CLKOB
	16		11	L16	PB20/SMRXD2/L1CLKOA
	14		12	N19	PB19/RTS1*/L1ST1
	12		13	N17	PB18/RTS2*/L1ST2
	10		14	P18	PB17/L1RQB/L1ST3
	8		15	N16	PB16/L1RQA/L1ST4
	6		CLK	W15	IRQ7*

Mictor 38		Logic Analyzer		Microprocessor	
Conn.	**Pin#**	**Pod #**	**Bit#**	**Pin#**	**Signal name**
J6	37	12	0	R17	PB15/BRGOUT3
	35		1	U18	PB14/RSTRT1*
	33		2	U17	PD15/LD8/L1TSYNCA
	31		3	V19	PD14/LD7/L1RSYNCA
	29		4	V18	PD13/LD6/L1TSYNCB
	27		5	R16	PD12/LD5/L1RSYNCB
	25		6	T16	PD11/LD4/RXD3
	23		7	W18	PD10/LD3/TXD3
	21		8	V17	PD9/LD2/RXD4
	19		9	W17	PD8/LD1/TXD4
	17		10	T15	PD7/LD0/RTS3*
	15		11	V16	PD6/LCD_AC/LOE/RTS4*
	13		12	U15	PD5/FRAME_VSYNC/RRJECT2*
	11		13	U16	PD4/LOAD_HSYNC/RRJECT3*
	9		14	W16	PD3/SHIFT_CLK/RRJECT4*
	7		15	V14	IRQ0*
	5		CLK	U14	IRQ1*

Related Literature	**Pub. Number**
Probing Solutions for Agilent Technologies Logic Analysis Systems	5968-4632E

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Ordering Information

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Product	Description
E5346A	High-Density Termination Adapter
E5346-68701	Kit of Five Mictor Connectors and Five Support Shrouds
E5346-63201	High-Density Right Angle Adapter
E5346-44701	High-Density Termination Adapter Support Shroud
E9584A Opt. #001	Motorola MPC 860/821 Inverse Assembler
B4620B	Source Correlation Tool Set
AMP PN 2-767004-2	AMP Mictor Connector (order from AMP)

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Printed in U.S.A. 12/99
5966-4165E

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