In-Circuit Testing of High Node Count Boards– Bigger is Not Always Better

White Paper

Abstract

The in-circuit test (ICT) engineer faces serious financial and technical challenges when testing more than 3500 nodes. Testing the entire board at one time with a single large tester and a fixture is the conventional approach, but results in expensive high node count testers and unproven high node count fixtures. Rather than adopt this "bigger is better" strategy, test engineers can intelligently split the board test in half and test it on two lower node count fixtures, using existing testers, standard fixturing and a standard process. This article compares these techniques on a real board.

Case Study

This article is based on a real in-circuit board test and fixture for a PCB with 5700 probable nodes, 126 vectorless test devices, with excellent Boundary Scan implementation, 2550 50-mil (unreliable) probe locations, and a production volume of 100 per day.

Bigger is Better?

To test the board using the "bigger is better" approach, one needs a 6500-node tester, one 5700-nail fixture with 2550 50-mil probes and a pneumatic gate. Several fixture vendors are now making these large fixtures. They have a lead time of 6 to 8 weeks, weigh up to 250 lbs., cost $75K, and are difficult to modify for engineering change orders (ECOs). The test time for a board this size on a conventional tester would be 100 seconds. Since there are many 50-mil probes, the retest rate would be high. The retest rate could be improved by cleaning the boards, but for many, this is not an acceptable option. Furthermore, the false failure rate would be high. Repair costs would skyrocket, given the higher rework costs for today's boards. Test development and debug would occur in a standard fashion and test coverage would be typical for ICT.

Divide and Conquer

The key to the "divide and conquer" strategy is to test the board twice on different fixtures using a single advanced 3500-node tester. Test development proceeds normally for the entire board and then the tests are intelligently split into two separate board volumes before the fixtures are designed. The splitting process can be almost entirely automated. (For the Agilent 3070 board test system, this process is described in the attached case study, "APG Agilent 3070 Split Fixturing Concepts," by APG Test Consultants, Inc.) The result: two fixtures that have identical power, digital disabling and Boundary Scan nodes and separate nodes for shorts, analog, Agilent TestJet, and digital tests. The nodes selected for the separate shorts tests will catch all shorts on adjacent pins of a device. Only trace shorts will be missed.

For the subject 5700-node board, the two fixtures contained 3300 and 3100 nodes. Since the two fixtures were less dense than one large single fixture, they were built with proven methods in 8 to 10 days, actuated by vacuum, with 1150 fewer 50-mil probes, and with greatly improved reliability and retest rates. If top-sided probes had been needed for the large board, the split board's reduced density might have allowed us to use equivalent bottom locations, thus reducing the number of top-sided probes. Further, today's generation of advanced testers boasts improved test times. If a second tester is available, parallel debug is possible, further reducing time to production. Finally, the split fixture concept dovetails with system-related fixturing, which provides simpler, lower-cost fixtures with improved reliability, as well as easier top-side probe implementation.

Summary

Splitting large boards and testing them twice on fixtures with under 3500 nodes makes good business sense. Costs and complexity of test do not scale linearly when node count is above 3500. As shown, two lower node count fixtures cost less, can be delivered faster, are more reliable and can be built with standard methods compared to a single large fixture. Testers with under 3500 nodes are cheaper and faster than 6000-node testers and total test times can actually be less, given the improved performance of the

less-dense fixtures and the speed of the new generation of testers. Test development time is minimized with software to automate this process, and the shorts tests will catch all shorts on adjacent pins of a device with only trace shorts being missed.

Projected Test Strategy Comparison

	Conventional 6500-node tester, one 5700-node pneumatic fixture	Advanced 3500-node tester, two 3200-node gated vacuum fixtures	Advanced 3500-node tester, two 3200-node system related fixtures [1]
System Cost	$700K - $1000K	$600K - $700K	$665K - $765K
Fixture cost (total)	$74K	$52K	$47K
Fixture weight (per fixture)	200 - 250 lbs	70 lbs	50 lbs
Fixture lead time	30 to 60 days	10 days	8 days
50 mil probes	2550	700	700
Top side probes	1000	Reduced (250)	Reduced and only on one top plate (250)
Fixture reliability	Poor, fair if boards are cleaned	good	Excellent
Fixture Induced Retest Rate [2]	20%	10%	5%
Beat Rate (boards/shift) [3]	204	182	217
Number of good boards failed per year [4]	2040	912	271
ECOs	Difficult	Easy	Easy
Debug	Standard	True parallel possible	Standard
Test Development	Standard	Standard plus 2 steps	Standard plus 2 steps
Missing Coverage	None	Non-adjacent shorts	Non-adjacent shorts

Notes:

1. A system-related fixture allows simpler board fixtures with improved accuracy. In this case, one fixture top (holder, top plate, support plate, Agilent TestJet MUX Boards, top-side probes) is used with both fixture bottoms.

2. Fixture-induced retest rate is deduced from standard tolerance stackup analysis of fixture. An excellent reference is Agilent Application Note 340-1. Note that no false failures from tester inaccuracies are accounted for.

3. Beat rate is calculated using the following assumptions:

   - Batch size = 100 boards per batch, fixture is changed between batches for split boards.
   - Test time = 100 seconds on conventional tester, 50 seconds on advanced tester.
   - Handling time = 20 seconds for gated and pneumatic fixtures, 10 seconds for system-related fixture.
   - Fixture change time is 2 minutes.
   - Test overlap is 5 percent on the split board.

   Single large fixture beat rate = ((Handling time + Test Time*(1 + Retest Rate))*Batch size + Fixture change time)/Batch size

   Two-fixture beat rate = ((2*Handling time + 2*(Test Time/2)*(1 + Retest Rate)* (1 + Test overlap))*Batch size + 2*Fixture change time)/Batch size

   The rates are then converted to boards per shift using an 8 hour shift.

4. These are the number of boards that will get sent to repair over the course of a year due to fixture-induced problems. The following assumptions are made:

   - Yearly volume = Number of boards per shift * 5 shifts per week * 50 working weeks per year
   - Boards will be sent to repair if they are retested more than once and still fail

   One can get a feel for the costs by then multiplying the number of boards by average repair cost per board. Some customers report this to be as high as $300 per board for some complex boards!

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APG Agilent 3070 Split Fixturing Concepts

The growing complexity of today's electronic circuit boards are pushing manufacturing and test to new limits. To successfully produce high node count boards of the best quality it is imperative that the electronics manufacturer identify new ways to measure and understand the manufacturing process. APG's split fixture process is an example of the innovation required to deal with the ever increasing complexity of tomorrow's manufacturing problems. This is an example of an 8300-node board that was previously tested on one fixture with limited test coverage. The test has now been developed on two separate fixtures with full test access at a reduced price with significant reduction in test development time.

As manufacturing processes mature and improve, high-node-count boards are becoming a viable solution for condensing and integrating multi-board systems into smaller and more efficient packages. The test methods used to maintain manufacturing process improvement must change to accommodate this increased complexity. Increasing available testhead resources will not completely eliminate the problem. Testing the 8300-node board on one fixture means longer fixture lead times (three times that of the standard five-day turn) and time-consuming test development and debug, ultimately resulting in loss of test coverage and increasing costs for a substandard board test product.

To successfully deliver a test application on two separate fixtures for a high node count board, a robust manufacturing process is required. In this split fixture example the board was initially developed assuming an unlimited number of testhead resources are available. The CAD data was translated using the standard APG translator "XC," an in-house translation solution. This is a highly configurable translator which quickly produces the required Agilent board output files as well as generating the appropriate mylar plots to be used with the bare board for physical nodal access evaluation. Additional steps were also taken to allow the use of APG's boardless fixturing process on the extremely dense board consisting primarily of fine-pitch double-sided BGA and surface mount technology. Program generation was then completed on the entire board to produce a baseline for test resource requirements for the complete board's circuitry. The next phase was a completely manual process for identifying circuit clusters which functioned together using the board schematics. This is the only manual step in the test development process.

After evaluating the board circuit description and completing the initial program generation, the process was taken over by a set of utilities which split the application in half. Each fixture maintains access to a common set of all power nodes, all Boundary-Scan chain nodes (13 chains consisting of 38 devices) and all digital test disabling nodes, in addition to the nodes required to perform the tests on the devices specific to each test program. The entire board must be able to be disabled on each fixture utilizing the common set of nodes.

To achieve access to the required nodes, the utilities gathered data for each "device.pin" and its respective node. The board_xy files were then automatically edited to change the attributes to no-access for each node where the utility deemed test resources were not required. Both nodal and device attribute sections of the board_xy files were changed to reflect that access was not available to nodes that were not being used to test the board on the associated fixture. Drilled alternate nodes that were not potential test resources in very dense 50-mil areas were also automatically removed from the fixture, reducing the initial 50-mil probe count by 1150 probes. This step alone significantly lowered the cost of the test fixtures. The utilities also analyzed digital devices that required Agilent TestJet and updated the appropriate TestJet entries in the board file. Analog nulltests were evaluated to ensure that each test that was not a nulltest in the initial development remained testable in at least one of the final test programs. The original libraries and board information were then used to develop the two sets of board and fixture files. This process was relatively trivial since the original board files that had already undergone the initial program development and compilation. The result was two separate fixtures, one with approximately 3300 nodes, 3800 wires containing 74 TestJet, and the other with 3100 nodes, 3600 wires containing 52 TestJet. Of the 8300 nodes, 2600 nodes on the board did not need test resources (single pin no-connects). Access was achieved on each of the remaining 5700 nodes between the two fixtures.

Each fixture has been manufactured using APG's newly developed linear vacuum sealing chamber design. This type of design reduces the weight of each fixture by an estimated 40 to 45 lbs. and represents a four percent reduction in cost per fixture. This also provides the safest environment for testing boards that are being powered using -48V at between 4 and 5 amps while allowing for complete visual access to the board being tested. The top gate contains no metal bars that can become loose or obstruct the view of the board, and it accommodates 6300 lbs. of evenly distributed downward atmospheric pressure to move the board on to an internally reinforced probe field with a completely linear motion. Each of the 700 to 800 50-mil probes per fixture are guided to achieve consistent successful registration with APG's two-piece guide blocks that are also machined to provide the bottom-side BGA support which is critical to prevent damage to sensitive BGA solderability.

Maintaining and continuing to improve this automatic Agilent 3070 split fixture process, along with APG's overall test application and fixturing processes, are the key to providing cost-effective, innovative solutions for Agilent 3070 board test. Combining programming and fixture fabrication expertise in one facility allows APG to experience process improvement and innovation daily.

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Printed in USA 2/00
5968-5467E

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