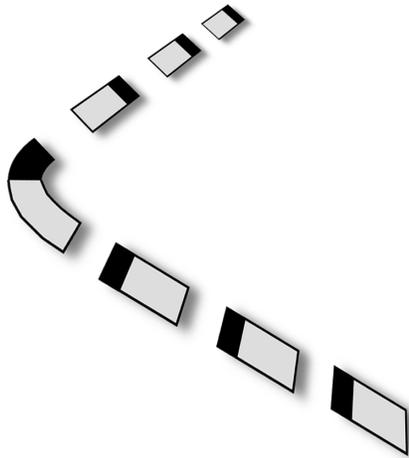
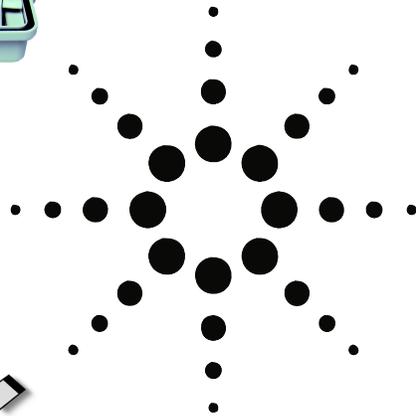


Jitter tolerance testing in an ATM environment

Product note



OmnibER
communications
performance
analyzer



It is often assumed that all the problems associated with ATM lie at or above the ATM layer. This is not always the case. For example, in today's high speed multi-technology transmission network, ATM cells are often carried in PDH, SDH or SONET networks. In such situations, physical layer jitter can occur on the ATM bearing signal and if ATM network equipment is not tolerant to this jitter, problems will occur at the ATM layer and above.

This product note discusses the nature of these problems and describes a method for testing an ATM network element's susceptibility to physical layer jitter up to 2.5 Gb/s.



Measuring jitter tolerance of high speed ATM network elements

Introduction

The physical layer jitter present in ATM traffic arriving from a SONET or SDH network element (NE) results from two primary sources:

- The “bit-stuff justification” process which is performed when a plesiochronous signal is mapped into the synchronous transport signal
- Pointer adjustments which compensate for asynchronous operation between different nodes within the SONET/SDH network.

The effect of jitter at an interface not sufficiently tolerant to this type of degradation is to introduce bit errors into the signal. The type of problem experienced in the network depends on where these bit errors occur in the signal. For example,

- Bit errors introduced into the PDH/SDH/SONET frame overhead may, if excessive, cause loss of frame with the consequential loss of the ATM cell stream.

- Bit errors which impact the header of a cell may cause loss of the cell (if the error is uncorrectable) or cause the header to be corrupted into another “correct” or “correctable” header value; if another virtual connection exists in which this corrupted cell’s VP/VC is valid, then the cell becomes misinserted in that connection.
- Bit errors which occur in the cell payload will have higher layer effects. Retransmission of data may result, adding to the probability of network congestion.

Testing methodology

There are established methods for measuring bit errors in PDH or SDH networks. Bit error testing is used to derive a bit error ratio (BER) which provides an indication of transmission quality. In addition, bit error checks, for example bit-interleaved-parity (BIP) checks, are used to alert network management to transmission problems. However, because ATM switches and multiplexers always terminate the physical layer while extracting ATM cells, measuring bit errors directly is not possible.

The solution is to measure jitter tolerance indirectly. This involves generating an appropriate ATM signal into a previously configured ATM virtual connection in the system-under-test and then observing the ATM impairments that result when physical layer jitter is added to the ATM test signal.

The kinds of impairment that can be anticipated are loss of cell, errored cells (defined as cells containing any payload errors) and loss of frame (although this has a lower probability since framing is usually tolerant of bit errors).

Note that correctable header errors are only detected and corrected by the NE itself and therefore cannot be observed externally. Cells with uncorrectable header errors are discarded by the NE so are viewed externally as cell loss in the test channel.

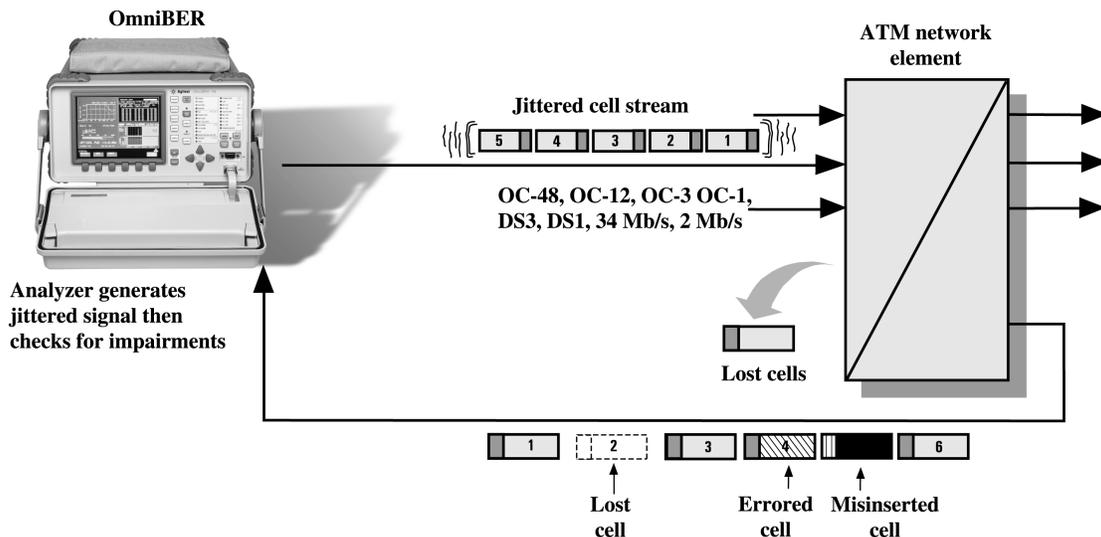


Figure 1. Setup for measuring jitter tolerance of an ATM network element

The Agilent solution

Agilent Technologies' OmniBER has the capability to add jitter to its internally generated ATM test source. This allows ATM and physical layer jitter to be tested simultaneously up to 2.5 Gb/s. Jitter can be generated and analyzed to Bellcore and ITU-T standards.

For ATM, the analyzer generates and analyzes test cells to ITU-T O.191. This provides the means for detecting cell loss and cell errors; the LOF alarm can also be identified.

Detecting these error modes has, in the past, meant manual tracking. However, OmniBER has an automatic jitter tolerance facility that allows an interface to be checked against a tolerance mask.

To establish the tolerance of an ATM NE, the analyzer generates jitter at different frequencies and at each frequency gradually increases the amplitude of the jitter until an error event occurs. A point is plotted on the tolerance graph corresponding to the jitter amplitude and frequency at which the event occurred. Once all points on the mask are plotted, an easy-to-interpret graphical representation of jitter tolerance is displayed (see Figure 2).

In detecting these error and alarm events, the analyzer applies its "TroubleScan" feature. In this mode, the analyzer systematically searches for appropriate detectable errors or alarms caused by the generated jitter, including those associated with ATM.

Performing the analysis

1. Configure the equipment as shown in Figure 1.
2. Set up a virtual channel connection or virtual path connection through the system-under-test (SUT).
3. Configure OmniBER to generate a PRBS at full rate on the virtual connection already set up in the SUT.
4. Configure the analyzer to analyze the PRBS received from the SUT (the VP/VC may be different).
5. Select the JITTER folder in the TRANSMIT screen and choose AUTO TOLERANCE; press RUN/STOP and observe the auto-tolerance graph plot.

Connecting an external printer or using OmniBER's graphics printer allows you to log the jitter auto-tolerance plot. Furthermore, you can store the results in text or bitmap form.

Instrument configuration

OmniBER must be configured to include an ATM cell layer option and jitter option 200. Additional options may include PDH/SDH/SONET and optical options (for ATM up to 2.5 Gb/s). For further information, refer to the OmniBER configuration guide.

Conclusion

As ATM networks migrate to higher rates, jitter impairments need to be fully characterised. With OmniBER, you have the capability to make output jitter, jitter tolerance and jitter transfer measurements, all with ATM mappings and all the way up to a full bandwidth of 2.5 G/bs.



Figure 2. Comparing an ATM NE's tolerance to jitter to GR-253



OmniBER communications performance analyzer

Offers a modular, upgradeable one-box solution for installation, commissioning, and field maintenance. This rugged, portable tester allows comprehensive functional testing of SDH, PDH and ATM equipment including jitter generation and test. A 3.5-inch disk drive eases results retrieval, test firmware upgrades, and analysis.

Related Literature

The complete global tester to 2.5 Gb/s (OmniBER 718) 5968-8740E

OmniBER 718 technical specification 5968-8335E

OmniBER 718 configuration guide 5968-8012E

OmniBER product note:
Measuring service disruption times in high-speed ATM networks 5968-9137E

OmniBER product note:
Verifying the policing functions in the ATM network 5968-9884E

OmniBER product note:
ATM performance testing 5968-9885E

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