Advanced Memory Buffer (AMB), Characterization of Timing and Voltage Specifications

Application Note

Introduction

Higher CPU speeds drive the need for higher memory bandwidth. For decades, CPUs have connected to the memory using a parallel synchronous bus, running at speeds up to a couple of hundred MHz. However, the speed of DDR2 technology, for example, limits the number of DIMMs in a system because of the multi-drop routing necessary. At the same time, other PC interfaces have successfully migrated to gigabit speed, multiple-serial connections. These overcome the technological problems at reasonable costs.

A new multiple serial interface, called Fully Buffered DIMM (FBD), applies this concept to memory interfaces. It uses Advanced Memory Buffer AMB) chips to connect the CPU to the memory at gigabit speeds.

The AMB chip connects directly to a DIMM using the current parallel synchronous interface. The short tracks between the memory and the buffer help to eliminate common problems with skew and signal integrity. This approach removes the immediate need to redesign memory chips, and opens the way to using terabytes of RAM, with currently available DIMMs - as well as those already on the road map.

As shown in figure 1, the interface between the memory controller and the memory is a point-to-point bus, with up to 24 lanes. In the first generation of FBD solutions, this runs at 3.2, 4.0 or 4.8 Gb/s. These speeds may soon double. The interface consists of 10 southbound lanes and12 to 14 northbound lanes. The southbound lanes transmit the commands from the CPU to the memory. The northbound lanes transport the data back to the CPU.

As each AMB chip buffers the signal for its neighbours, the north and south ports are implemented as TX and RX. Because each lane is differential, an AMB chip can have up to 96 pins running at gigabit speed[1].

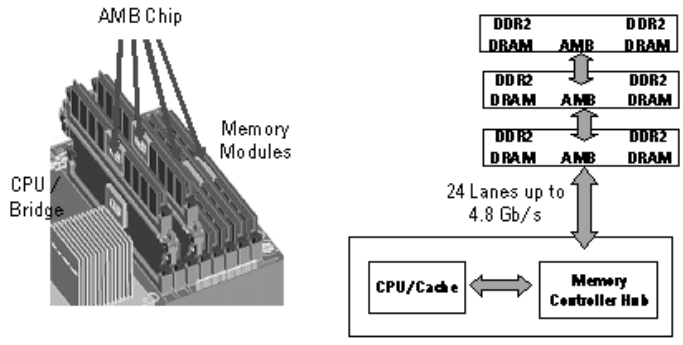


Figure 1: FBD architecture

AMB chip specification

Figures 2 and 3 are taken from the AMB Reference Specification[3] available at the time of writing. The diagrams show the eye specification, or eye mask, for the electrical signals, for both input (RX) and output (TX). These apply to any lane, operating northward or southward.

The TX output is specified with a programmable driving strength and de-emphasis. De-emphasis means the bit after a transition (a transitional bit) is driven with higher amplitude than a bit that has the same value as the preceding bit (a de-emphasized bit). De-emphasis compensates for the degradation of frequency response and losses in the channel, which in this case is the motherboard. This compensation reduces the jitter caused by Inter-Symbol Interference (ISI) and provides better eye openings of the transmitted signals at the RX. This improves the jitter performance for the whole channel. Apart from compensating for jitter, this also improves the power consumption.

The RX input is designed to work with a much smaller eye than transmitted by the TX. This allows for amplitude loss in the channel and the deficiencies of the jitter compensation.

In the time domain, the TX and RX signals are defined by a minimum eye opening Teye_min, where:
Teye_min + total jitter = 1UI
where UI is the unit interval. For the TX output, the minimum eye opening is 0.7 UI. At the RX input, it is 0.6 UI.

Voltage specifications are provided for the differential signals. The TX output must be between a minimum and maximum amplitude, taking the attenuation ratio of the de-emphasized bit into consideration. The minimum amplitude for TX is 520 mV. This corresponds to 350 mV when de-emphasized by 3.5 dB. The minimum input swing for RX is defined as 170 mV.

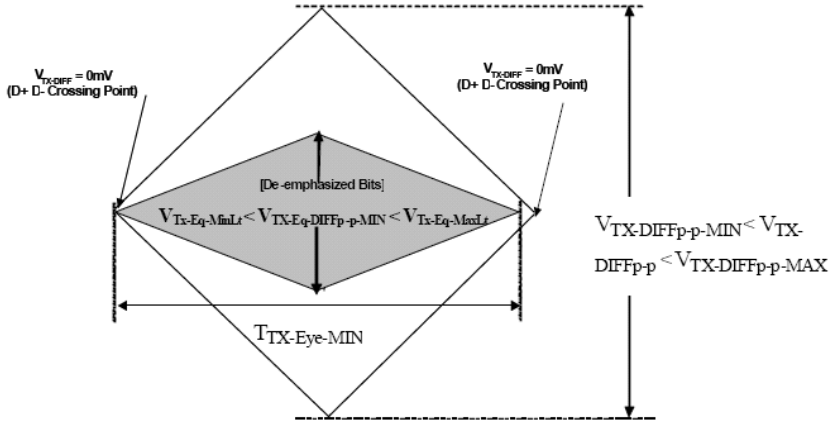


Figure 2: AMB TX Output Eye Specification

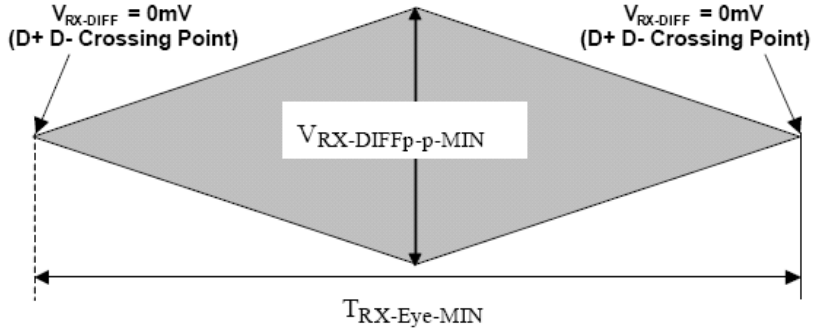


Figure 3: AMB RX Input Eye Specification

FBD/AMB test solution summary

Figure 4 shows the variety of test solutions provided by Agilent Technologies for testing the various layers of FBD and AMB functionality. Apart from verification and characterization, there are solutions for system level test and high volume manufacturing test. This document focuses on characterizing the timing and voltage parameters of the AMB chip, using the Agilent 81250 ParBERT system, with the 86100C Infiniium DCAj Wide Bandwidth Oscilloscope. Characterizing physical layer parameters means evaluating the electrical parameters of the high-speed inputs and outputs of the AMB chip, and comparing them with the references[3], [4].

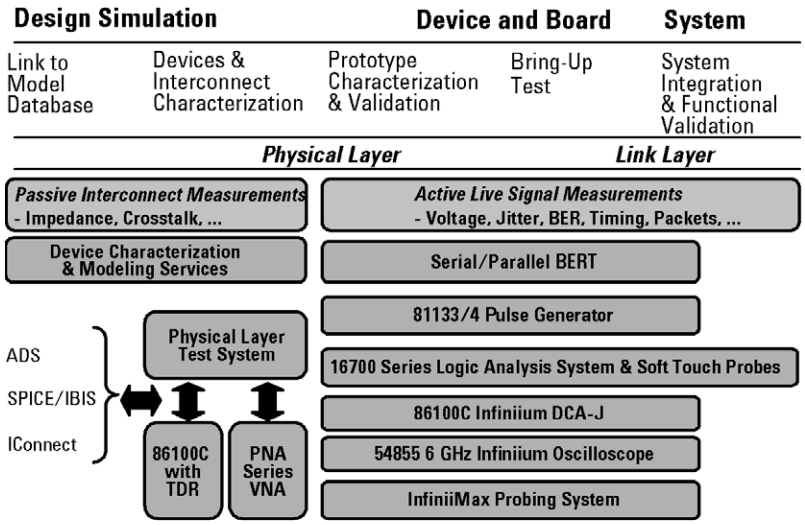
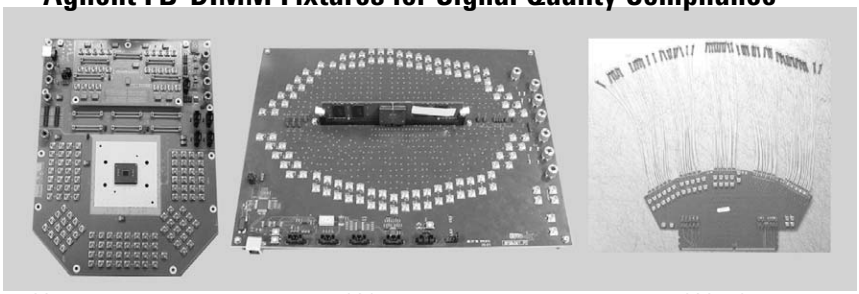


Figure 4: Agilent's test solutions for FBD / AMB

AMB chip fixturing

Apart from the test equipment detailed below, testing the characteristics needs a reliable connection to the AMB chip under test.
For reliable signal measurements, properly designed transmission lines are important. These need controlled impedances of 50 or 100 differential, and minimized losses. Agilent provides three test fixtures (see figure 3). These allow testing the bare chip (N4235A), of the AMB on a DIMM (N4236A), or of the AMB system channel (N4238A).



N4235A AMB PArametric PArametric Probe **TestN4236A DIMM PArametric Test** **N4238A Slot**

Figure 5: Test fixtures

86100C Configuration

The 86100C DCAj is the most precise signal-integrity analysis tool currently available. It has the lowest amplitude noise floor, the lowest intrinsic jitter, the best jitter sensitivity and, with Option 200, it includes the most accurate jitter analysis algorithms available[7].

To analyze differential electrical signals, the best receiver module is the 86117A with - a 50 GHz bandwidth module.

The DCAj needs a clock signal trigger. If a clock signal is not available on the device under test, we use the 83496A-100 clock recovery circuit with the standard configuration. We can set this for any data rate between 50 Mb/s and 7.1 Gb/s (up to 13.5 Gb/s with Option 200). We can set the clock recovery loop bandwidth at either 270 KHz or 1.5 MHz (or from 15 kHz to 10 MHz with Option 300).

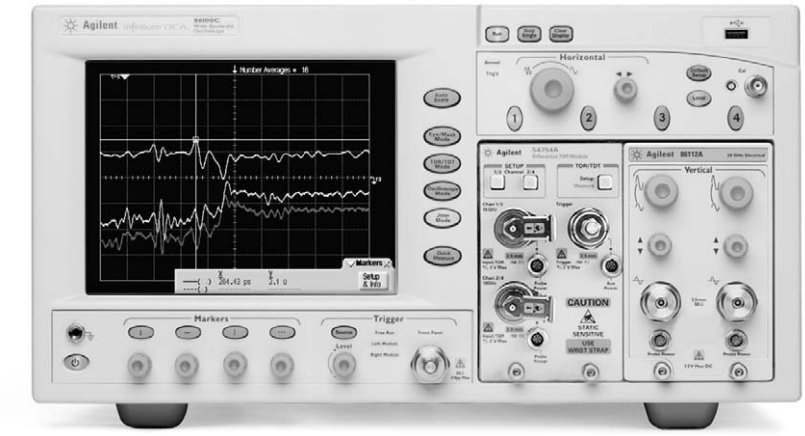


Figure 6: 86100C DCAj

86100C DCAj system

- 86100C Mainframe with Option 001 and Option 200 (Option 201 is recommended, but not required).
- 86117A dual electrical receiver module (86112A provides a lower cost alternative but provides 20 GHz band width only. Alternatively the 86118A provides up to 70 GHz band width and with option HO1 a skew adjust between the two channels.)
- 83496A-100 clock recovery module.

81250 ParBERT Configuration

The 81250A ParBERT system offers the highest flexibility for configuring multiple channels to test multiple lanes or setup multiple de-emphasis signals. For the first generation of AMB, the 7 Gb/s modules should be sufficient. There is always the possibility to upgrade to 13.5 Gb/s.

The 7/13.5 Gb/s configuration contains two clock groups:
The first clock group contains three 7/13.5 Gb/s Pattern Generators and one Analyzer. We need at least two generators. The third generator can be used, for example, for crosstalk testing.
The AMB chip needs a reference clock at the frequency of the data rate divided by 24. As this is not binary, we need to do this with a second clock group equipped with a generator module.

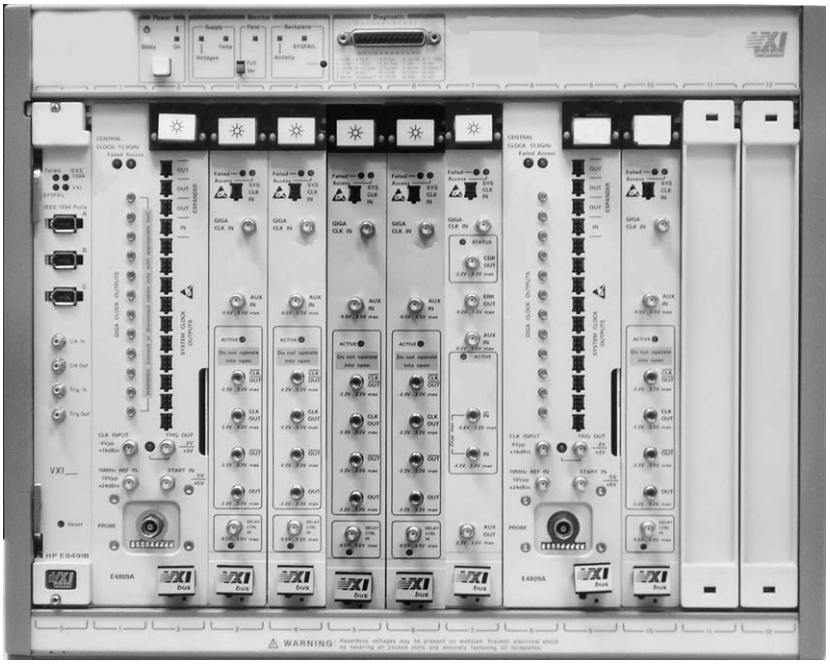


Figure 7: 81250A ParBERT configuration

7/13.5 Gb/s ParBERT system
- 1 x 81250A ParBERT with #013 Firewire and #149 Frame
- 1 x E4875A User Software
- 2 x E4809A 13.5 GHz Clock
- 4 x N4872A/74A 13.5 G/7 G Pattern Generator Module
- 1 x N4873A/75A 13.5 G/7 G Analyzer Module.

Additional equipment:
- 33250 Arbitrary Waveform Generator
- 4 x power supplies
- PC with USB connections and Python Software installed
- N4235A AMB Fixture

How to Setup the Equipment

For the test we need to setup:
1. Clock: We configure the ParBERT for two clock groups. The clock group with the single data generator is the clock source. We load this generator with an alternating pattern of 12 '0's and 12 '1's. This provides a reference clock with frequency at a 24th of the data rate.

We connect the data output to SCK/SCKn of the fixture. We also connect the clock outputs to the external clock input of the other clock group, and to the trigger input of the oscilloscope.

AMB chips use spread spectrum clocking (SSC), which we do not deal with in this application note. For SSC testing we would need an external signal generator (not in the equipment list) to provide the SSC modulated clock to both clock groups. For more details see reference [5].

2. We need to stimulate at least two of the lowest three southbound lanes to the AMB. We use two generators driving the normal and inverted input to force electrical idle with a 0 V swing. We split the signals with two power dividers to supply them differentially to PS0 and PS1: This lets us drive two lanes with two generator channels.

3. For jitter tolerance testing, we split the output of 33250A with a power splitter, and feed each signal to the delay control input of the generators supplying PS0 and PS1.

4. We can connect the third generator differentially to any other southbound lane. This lets us measure the lane or create crosstalk.

5. We perform all analysis on the differential signals. We connect the ParBERT analyzer to lane SS0 and the two inputs of the DCAj to SS1. We analyze the differential signal by subtracting one signal from the other.

6. A PC with Python software can read and write the registers in the AMB over USB and the SMBus. The documentation of the E4235A fixture provides some basic information on this.

7. We need to power the fixture with 3.3 V, 1.8 V, 1.5 V and 0.9 V. For this, we need to build a harness with banana jacks to plug into the fixture.

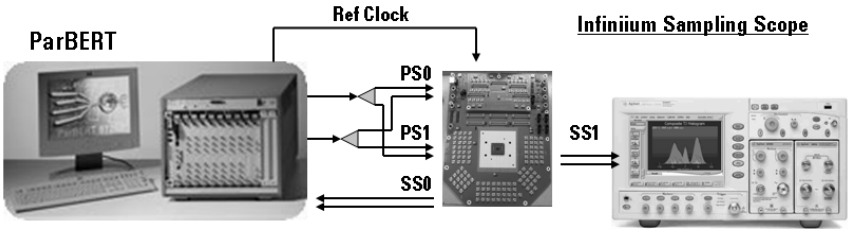


Figure 8: Schematic of Test Setup

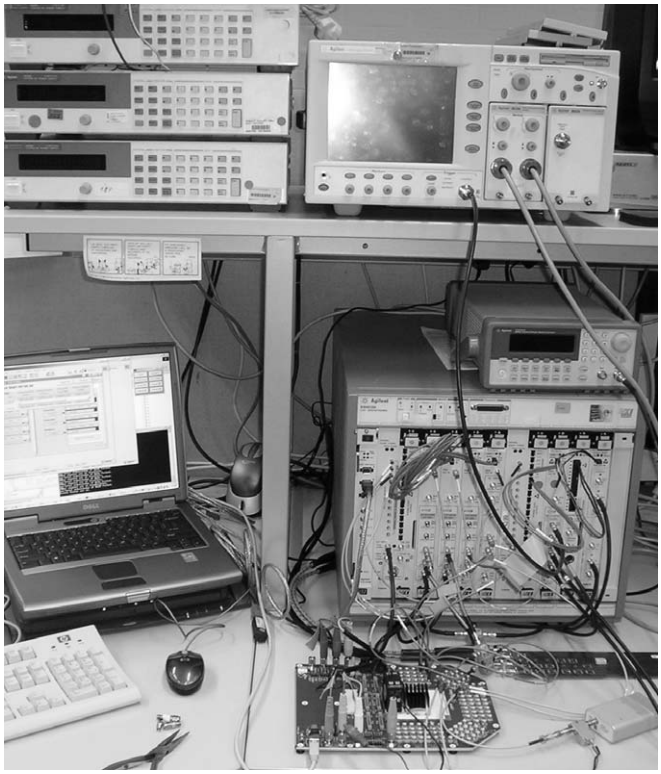


Figure 9: Equpiment Setup

How to Set-Up the AMB Test

Frequency
All the tests described here use 3.2 Gb/s data rate, but the setup could just as easily be used at 4.8 Gb/s (9.6 Gb/s with 13 G)

Levels into southbound lanes:
The basic levels are LOL = 0 V, HIL = 0.7 V. This gives a differential level of 1.4 Vpp. The termination voltage, Vt, is set to 0 V.
For PS0 and PS1 set HIL to 1.4 V.

Set Analyzer:
The termination is 0.55 V and the threshold is 0.55 V if single ended, or 0 V if differential.

The test bits:
Figure 10 shows the bit flow needed. After electrical idle we need to go through TS0, TS1 and TS2 before the AMB is in the right mode to loop the incoming bits. Figure 11 shows the ParBERT sequence for stepping through the states. There is one block for each state. Once started, the electrical idle is sent to the AMB. With the event handling assigned to the CMD radio buttons, we can now transition from block to block.

Feedback:
A Python script reads the AMB internal status register (1,64h), this lets us verify the correct recognition of each state[2]. With the DCAj connected to SS1 we can monitor the AMB output, and check the signal when entering the training and all following states.

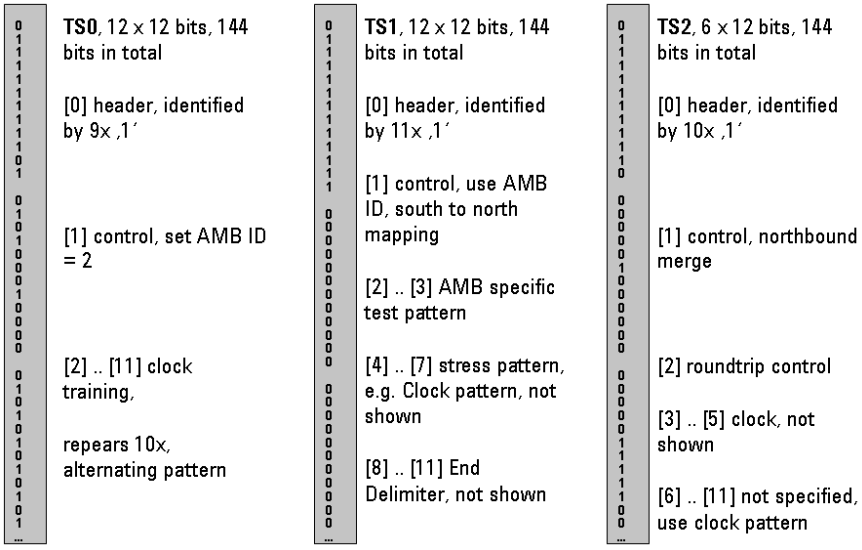


Figure 10: Training Sequences Details

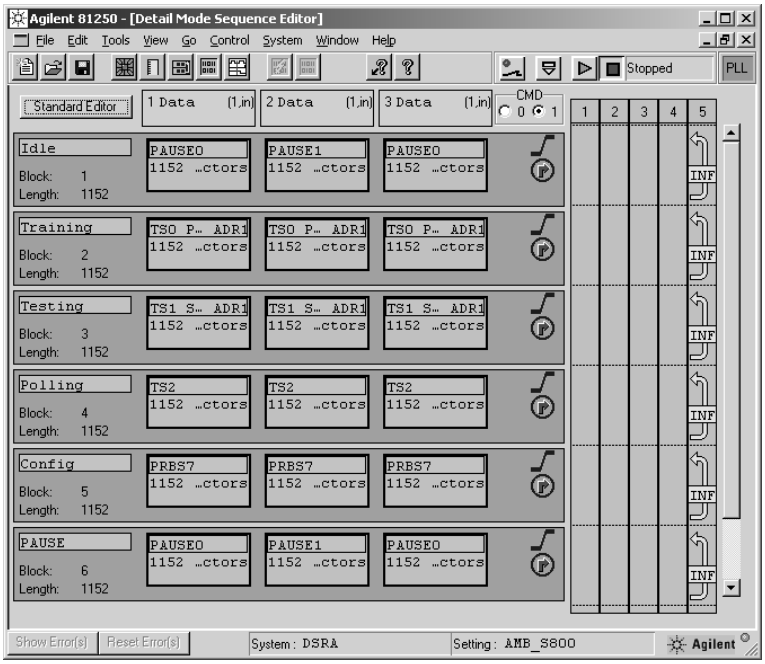


Figure 11: Sequence for State Stepping

How to prepare for Characterization

The difference between characterization and function test is the need for an almost infinite length pattern to and from the AMB to make the measurements. We adapt the ParBERT sequence, so after the initialization with idle and the training sequences, it provides a PRBS pattern in an infinite loop. We do not use the events any more: each training segment loops long enough so the AMB recognizes it properly. Also, we now include the ParBERT analyzer in the sequence. Block 5 provides synchronization to the PRBS pattern; Block 6 does the BER measurement. We use the sequence shown in figure 12 for all the following DCAj and BERT measurements.

We distinguish between two types of measurements: the TX and the RX tests. The TX test keeps the input signal mostly the same for all tests while the analyzing tool moves within the output signal. For RX testing, we vary the voltage and timing parameters of the input signal, while watching the BER of the output signal. The BER changing from 0 to 1e-9 is a good indicator of the point at which the input signal is forced to the limit of the input circuitry. We get themost accurate results by using the DCAj to calibrate the input signal. However, these measurements are time-consuming, as they need much reconnecting

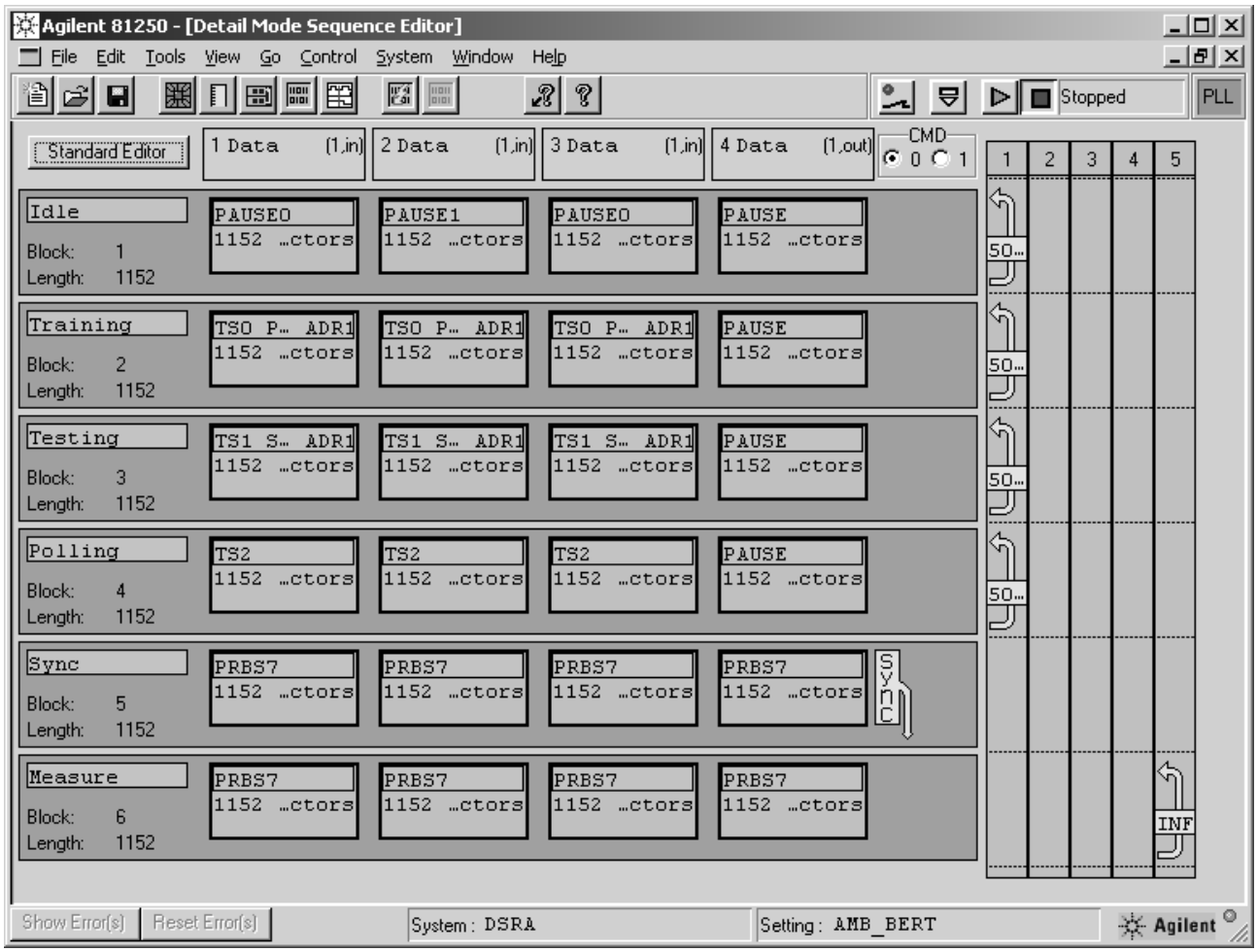


Figure 12: 81250A ParBERT Sequence for Waveform, BER, Timing and Jitter Test

TX Results, Waveform Measurements

We stimulate PS0/PS1 as described earlier with the verification sequence; then we look at SS0/SS1.
The DCAj has many analysing capabilities in Oscilloscope and Eye/Mask mode to measure parameters such as the transition time automatically.

The DCAj also provides a one-button jitter mode which breaks the jitter down into extrapolated Tj, Rj, Dj(δ-δ), DDJ(p-p), DCD and ISI in a couple of seconds. Figure 13 shows a screen shot of the jitter measurement on the SS1 output.

As described earlier, the de-emphasis of the AMB outputs avoids or reduces ISI jitter by reducing output amplitude if a bit is stable for two or more cycles, and driving transitional bits with a higher amplitude. For de-emphasis the AMB outputs can be set to 0 dB, 3.5 dB, 6 dB or 9.5 dB. We use a Python script to write this into AMB register 1,54h.

We connect a 25 cm long backplane providing 50Ω transmission lines on FR4 material, differentially to the AMB output. This creates an ISI jitter of 22 ps at the data rate and pattern configured. We connect to the DCAj to the far end. From left to right, figure 14 show the eyes with 0 dB, 3.5 dB and 6 dB de-emphasis. The 3.5 dB setting shows the most open eye.

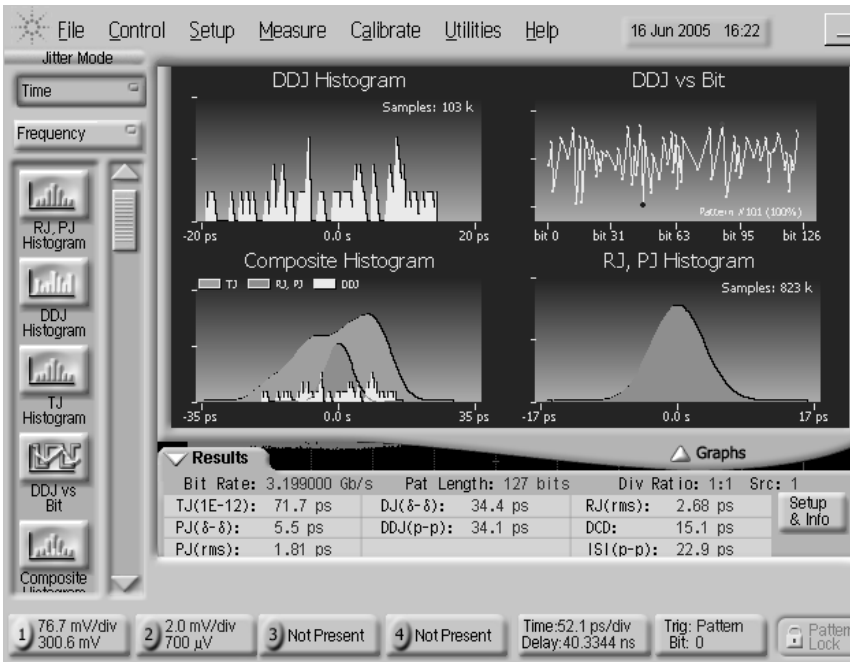


Figure 13: Jitter Measurement with 86100C

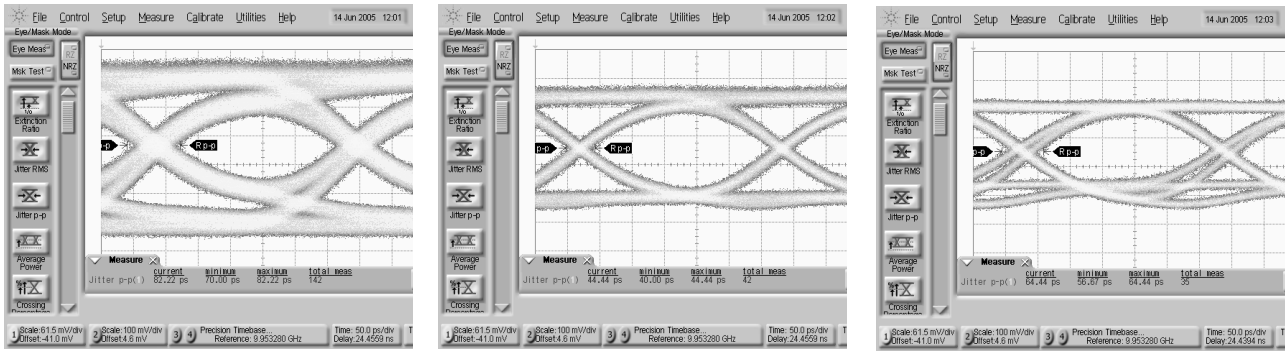
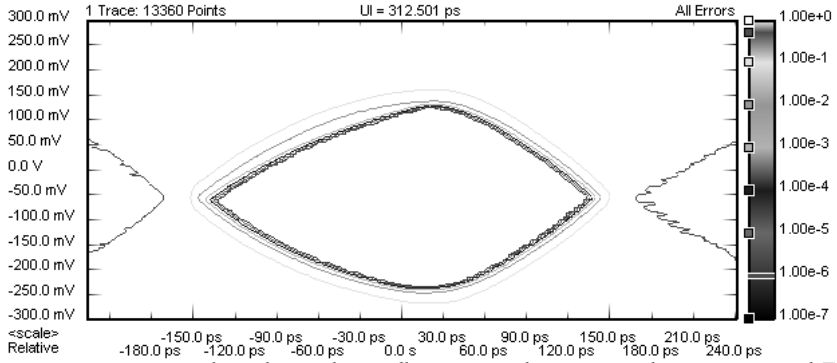


Figure 14: TX output signal for De-emphasis set to 0dB, 3.5dB and 6dB (left to right)

TX Results, BER & Timing Measurements

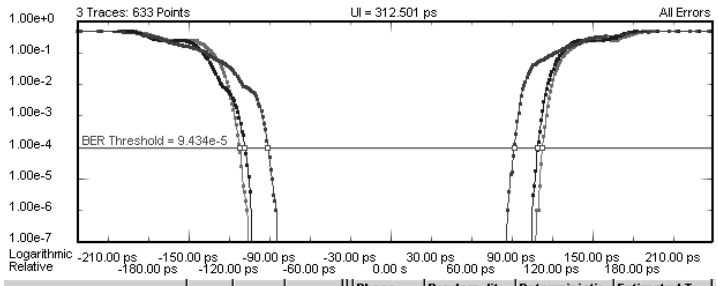
The 81250 ParBERT Analyzer has a differential connection, which allows analysis of the true differential signal. Figure 15 is the eye opening taken from the SS0 lane, with de-emphasis set to 3.5 dB.
The classical BERT scan, which is called Output Timing Measurement in the ParBERT, sweeps the sampling point over time and gives a graph within a couple of seconds. Apart from the graph, there is also a table giving numerical values for Phase Margin, Rj, Dj and extrapolated Tj. Figure 16 shows this BERT scan for the same de-emphasis settings used for figure 14. Again, the de-emphasis of 3.5 dB provides the most open eye and a minimum value for Dj.
The time to perform a BERT scan depends heavily on how low the BER shall be tested. The Tj at 1e-12 is always an extrapolation, as on the DCAj. For a BER less than 1e-12, the measurement will last many hours.

The Fast Total Jitter Measurement (FTM), shown in figure 17, uses a more efficient method. The FTM is the only tool that measures BER down to 1e-12 in the fastest possible way [8].



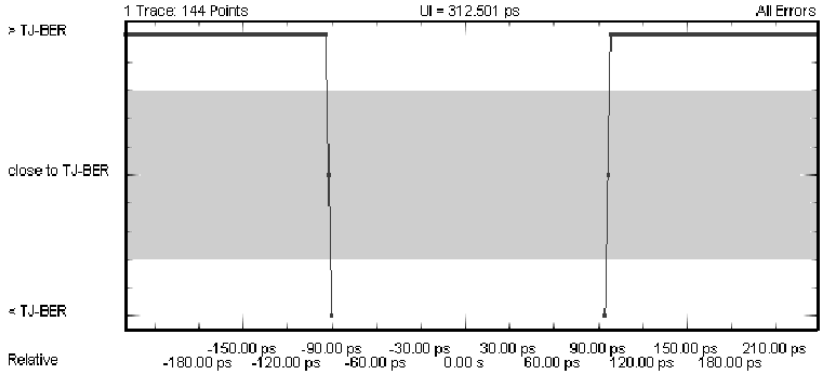
Port/Terminal	Show	Color	Copied	Time Eye Opening	Threshold Eye Opening	Optimal Sample Threshold
Measurement				(Rel. Time)	(Abs. Volts)	(Abs. Volts)
[4] Data				266 ps	360 mV	-55 mV
[4:1] Data0	☑			266 ps	360 mV	-55 mV

Figure 15: Differntial Eve Opening for De-emphasis 3.5db



Port/Terminal	Show	Color	Copied	Phase Margin	Random Jit... RMS	Deterministic Jitter	Estimated T... Jitter
Measurement				(Rel. Time)	(Rel. Time)	(Rel. Time)	(Rel. Time)
[4] Data				183 ps			
[4:1] Data0	☑			183 ps	5.39 ps	90.7 ps	165 ps
Measurement as of 06/21...			X	(Rel. Time)	(Rel. Time)	(Rel. Time)	(Rel. Time)
[4] Data (Copied)			X	218 ps			
[4:1] Data0 (C...	☑		X	218 ps	4.89 ps	59.7 ps	127 ps
Measurement as of 06/21...			X	(Rel. Time)	(Rel. Time)	(Rel. Time)	(Rel. Time)
[4] Data (Copied)			X	225 ps			
[4:1] Data0 (C...	☑		X	225 ps	4.65 ps	53.5 ps	117 ps

Figure 16: Output Timimg Measurement for De-emphasis to ObB (top), 3.5dB (bottom) and 6dB (middle) at ISI backplane



Port/Terminal	Show	Color	Copied	Total Jitter Peak to Peak	Total Jitter Uncertainty	Total Jitter BER Threshold	Phase Margin
Measurement				(Rel. Time)	(Rel. Time)		(Rel. Tim...
[4] Data				128 ps	5.66 ps	1E-012	185 ps
[4:1] Data0	☑			128 ps	5.66 ps	1E-012	185 ps

Figure 17: Fast Total Jitter Measurement for De-emphasis 3.5dB

RX Results: Jitter Tolerance

The RX measurements work by changing the input signal until it causes stress to the AMB input circuitry. We watch the BER of the AMB output signal. An increase in the BER signals that the input is no longer working properly.

In the case of the jitter tolerance measurement, we add sinusoidal jitter to the input signal. We do this by connecting the 33250A Arbitrary Waveform Generator to the delay control input of the ParBERT generator. We use a power splitter to provide the sinusoidal signal to both generators supplying the data signal to the PS0 and PS1 lane.

The amplitude of the sinusoidal signal defines the peak-to-peak deviation of the data edge, which in turn defines the peak-to-peak jitter. We increase the amplitude of the sinusoidal signal until the BER reading on the ParBERT analyzer changes from 0 to less than 1e-9.
The delay control input provides a typical conversion gain of 400 ps/V. We use this value to convert the amplitude reading into the applied jitter. We also need to consider that the power splitter halves the amplitude.
The more accurate but more time-consuming method is to verify the input signal by reconnecting to the DCAj and measuring the eye opening (as shown in figure 19).
For a complete jitter tolerance measurement we need to repeat at this at various jitter frequencies. Finally, we put the measured data in a spreadsheet, for visualization.

Figure 18 shows the results we got from SS0. The figure provides two curves: one for the case where we connect the generator directly to the AMB input (without ISI), the other when using the ISI backplane mentioned earlier. What is most notable is that a relatively small amount of ISI reduces the tolerance to sinusoidal jitter significantly.

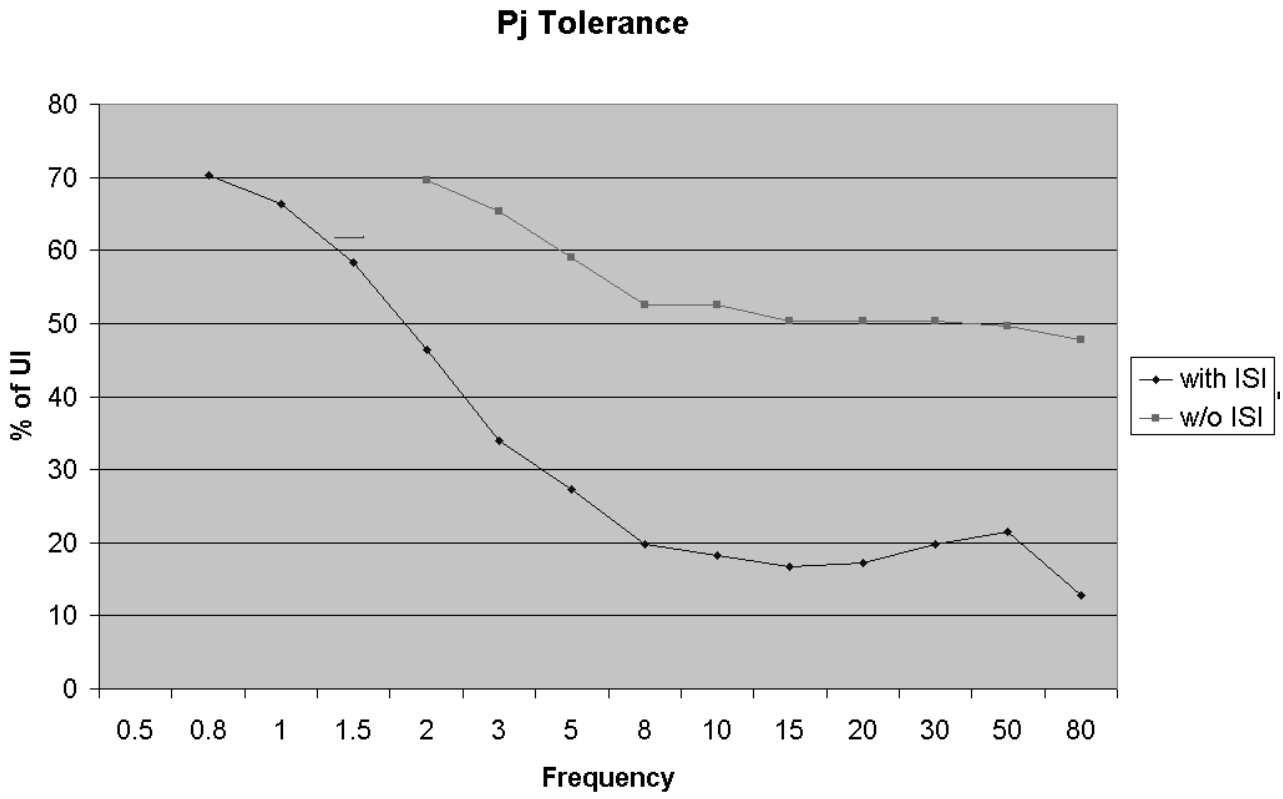


Figure 18: Jitter Tolerance Test using sinusoidal jitter with and without ISI (22ps)

RX Results, Receiver minimum Input Eye

Here we first verify the specification for the minimum input signal. Then we figure out the absolute minimum signal with which the device will work. From figure 3, the minimum input signal is 170 mV swing at 0.6 UI. This specification applies to the pin of the AMB.

Before we start with the RX minimum input signal measurements on the AMB, we need to measure the signal degradation in the test jig. The N4235A test fixture is designed for very clean impedance matching. However, we cannot neglect the losses from the FR4 material. These losses degrade the signal amplitude.
We need to determine this degradation and compensate the voltage settings accordingly. To measure the degradation, the N4235A provides a 4 inch test line. We stimulate this with a ParBERT generator and measure the signal with the DCAj. We compare the signal running through the test line with the signal that bypasses it.
As we will use transition time converters for signal conditioning later, we compare the amplitude degradation once for the fast signal and once for the converted signal. We found an amplitude loss of 15% for the fast signal, and 20% for the converted signal. In both cases, we lose 5 ps eye opening when running through the test line. We use these values to adjust for the measurements that follow.

To create the signal according the eye mask, we connect the ParBERT generator via the 150 ps transition time converter to the DCAj input. On the DCAj we create the mask according figure 5 (initially, we ignore the corrections needed for the degradation caused by the fixture).The power dividers divide the AMB input signal by a factor of 4. The DCAj measures single ended, so the equivalent voltage is 85 mV single ended, or 340 mV before the divider. We set the ParBERT generator levels to get a signal on the oscilloscope with 340 mV amplitude.

The BER reading must be 0. Theoretically, we should wait for 1000 seconds with no errors to verify the input will work for BER less than 1e-12 with a confidence level of 95%[6].

Then we enable the delay control and set the jitter modulation to get an eye opening of 187 ps, as shown in figure 19. Now, before we connect to the AMB input, we need to adjust for the signal degradation we measured. We increase the amplitude by 20% and reduce the jitter modulation by 5 ps.

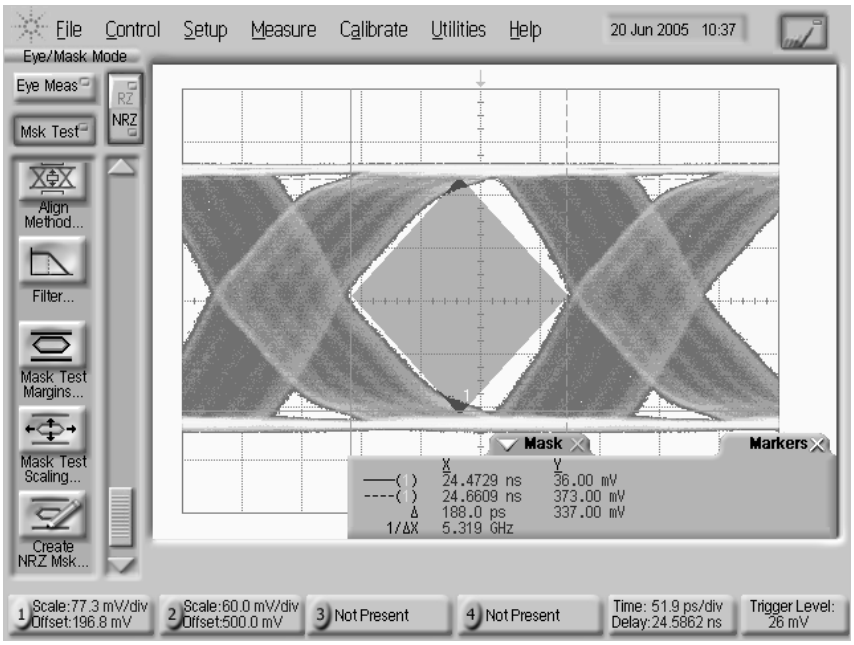
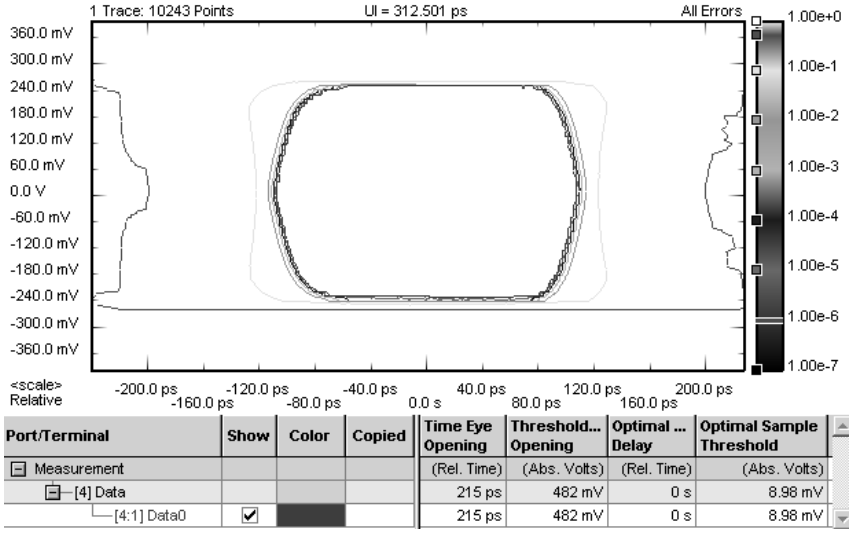


Figure 19: Receiver min. Input Signal measured with 86100C DCAj, mask defined according [3], with 150ps converter

To verify the absolute minimum amplitude we remove the transition time converters. With the jitter modulation turned off, we reduce the amplitude of the data signal going to PS0/PS1 by decreasing the HIL of the generators until the BER figure increases from zero. We increase the HIL again by roughly 5 mV so the BER reading is back to zero. Then we increase the sinusoidal jitter modulation until the BER shows the first failures. Again we decrease so the BER is zero again.

Now we verify the input signal by connecting differentially to the BERT analyzer, as shown in figure 20. As we measure this before the power dividers, we need to divide the voltage readings by 4 and adjust for 15% degradation. We calculated the absolute minimum input signal at the AMB pin as 105 mV at an eye opening of 68%.



Port/Terminal	Show	Color	Copied	Time Eye Opening	Threshold... Opening	Optimal ... Delay	Optimal Sample Threshold
Measurement				(Rel. Time)	(Abs. Volts)	(Rel. Time)	(Abs. Volts)
[4] Data				215 ps	482 mV	0 s	8.98 mV
[4:1] Data0	☑			215 ps	482 mV	0 s	8.98 mV

Figures 20: Receiver's absolute minimum input Signal measured with ParBERT Eye Opening Measurement

Conclusions

Together, the ParBERT and the DCAj have proven to be efficient tools for verifying and characterizing the AMB chip. The N4235A is a reliable fixture, with good performance for accurate verification and measurement.

References

[1] FB-DIMM Draft Specification: Architecture and Protocol, JEDEC JESDxx-x Proposal, March 2005

[2] FB-DIMM Draft Specification: Advanced Memory Buffer (AMB) , JEDEC JESDxx-x Proposal, October 2004

[3] FB-DIMM Draft Specification: High Speed Differential PTP Link at 1.5V JEDEC JC-16-04-xx Proposal, December 2004

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N4902B 7 Gb/s Serial BERT Datasheet	**5989-0399EN**
Jitter Solutions Brochure	**5988-9592EN**
Jitter Tolerance Testing with 81250 ParBERT	**5989-0223EN**
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Fast Total Jitter Test Solution Application Note	**5989-3151EN**
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Agilent ParBERT 81250, Parellel Bit-Error-Rate Tester Product Overview	**5968-9188E**
Jitter Tolerance Testing Agilent ParBERT 81250 Platform Application Note	**5989-0223EN**
Physical Layer Testing of Passive Optical Network Modules Application Note	**5898-3481EN**

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