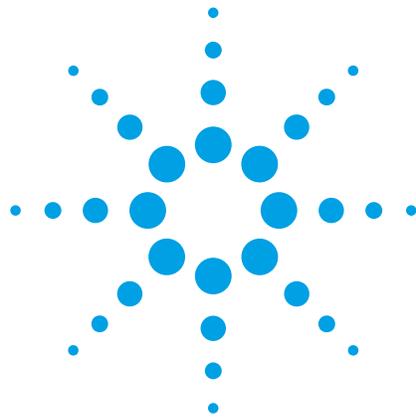# How to characterize the Physical Layer of the Mobile Industry Processor Interface (MIPI D-PHY)

Application Note

- Fast results needed when new ASIC comes out of fabrication

- Medium complex digital chips

- Performance of CDR, clock system and jitter tolerance

- GO - NO GO testing, some quantitative results

- Extrapolation to performance testing

Agilent Technologies

Introduction

MIPI D-PHY is the standard for a serial bus used in battery operated equipment to connect high data capacity devices like the camera module. Because of its capacity, D-PHY is also selected by companies such as NXP as the BB interface for WiMAX (and other high data rate formats) radios.

One thing you should know about MIPI D-PHY is that it operates in two modes, low power/low data rate (max 20Mbit), and a high data rate mode. The difference between the two is that the low power mode is electrically defined as a single ended, standard CMOS level: signaling and the high data rate is differential LVDS. The transition between modes is dynamic and is one of the critical areas that needs to be tested.

With the ParBERT Agilent Technologies, Inc. offers an instrument that allows the designers and manufacturers to stress the MIPI D-PHY receiver, i.e. all the standard pulse/data generator features needed (edge control, timing offset, etc). Special to the interface is the switching mode: the ParBERT can generate the control sequences and force the bus through the low to high speed transition (and vice versa).

Figure 1: Agilent 81250 ParBERT (Parallel Bit Error Ratio Tester)

MIPI D-PHY Standard and Implementation

A PHY can contain the following electrical functions: a high-speed transmitter (HS-TX), a high-speed receiver (HS-RX), a low-power transmitter (LP-TX), a low-power receiver (LP-RX), and a low-power contention detector (LP-CD). A PHY does not need to contain all electrical functions, only the functions that are required for a particular PHY configuration. Figure 2 shows the complete set of electrical functions required for a fully featured PHY transceiver.

Figure 2: Electrical Functions of a fully featured D-PHY transceiver

The HS transmitter and HS receiver are used for the transmission of the HS data and clock signals. The HS transmitter and receiver use low-voltage differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The LP transmitter is a push-pull driver and the LP receiver is an un-terminated, single-ended receiver.

The signal levels are different for the differential HS mode and the single-ended LP mode. Figure 4 shows both the HS and LP signal levels respectively on the left and right sides,. The HS signaling levels are below the LP low-level input threshold so that the LP receiver always detects logical low on HS signals. All absolute voltage levels are relative to the Ground voltage at the transmit side.

A lane switches between low-power and high-speed mode during normal operation. Bidirectional lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enabled and disabled events do not cause glitches on the lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes are smooth and always ensure a proper detection of the line signals.

The HS receiver is a differential line receiver. It contains a switchable parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. A simplified diagram of an example implementation using a PMOS input stage is shown in Figure 3.
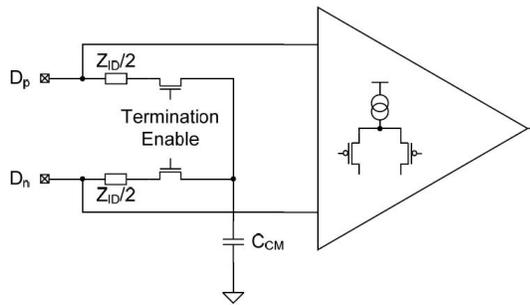
Figure 3:HS Receiver implementation including switcheable termination

The differential high and low input threshold voltages of the HS receiver are denoted by VIDTH and VIDTL. VILHS and VIHHS are the single-ended, low input and high input voltages, respectively. VCMRX(DC) is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its Dp and Dn input signal pins when both signal voltages, VDP and VDN, are within the common-mode voltage range and if the voltage difference of VDP and VDN exceeds either VIDTH or VIDTL.

The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference ΔVCMRX(HF) and ΔVCMRX(LF). During operation of the HS receiver, impedance ZID termination is required between the Dp and Dn pins of the HS receiver. ZID shall be disabled when the module is not in the HS receive mode. When transitioning from low-power mode to HS receive mode the termination impedance shall not be enabled until the single-ended input voltages on both Dp and Dn fall below VTERM-EN. To meet this requirement, a receiver does not need to sense the Dp and Dn lines to determine when to enable the line termination, but the LP to HS transition timing allows the line voltages to fall to the appropriate level before the line termination is enabled.
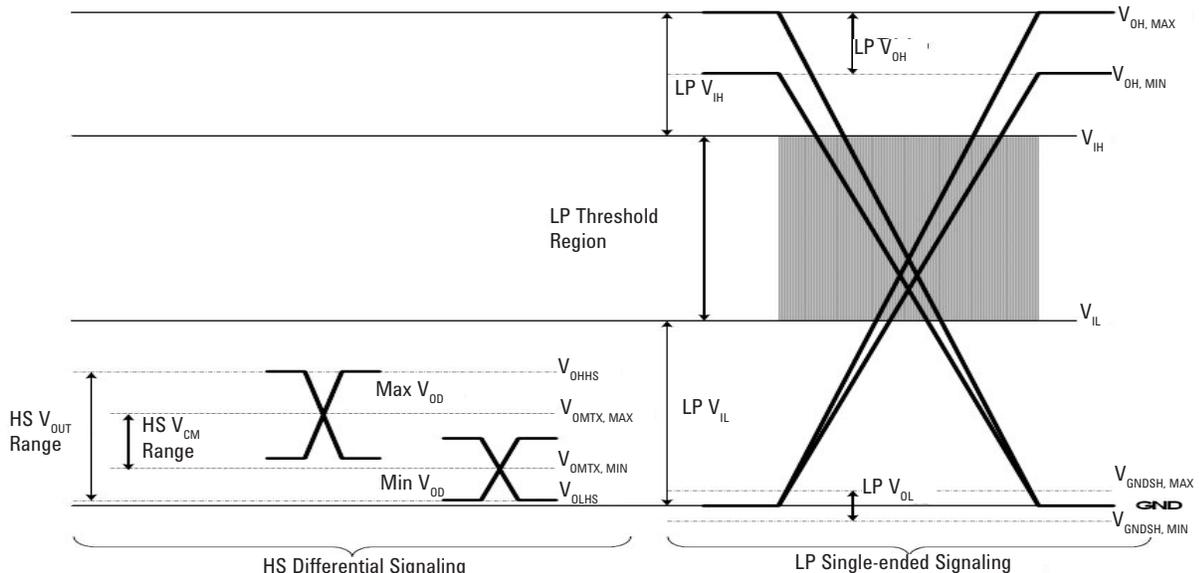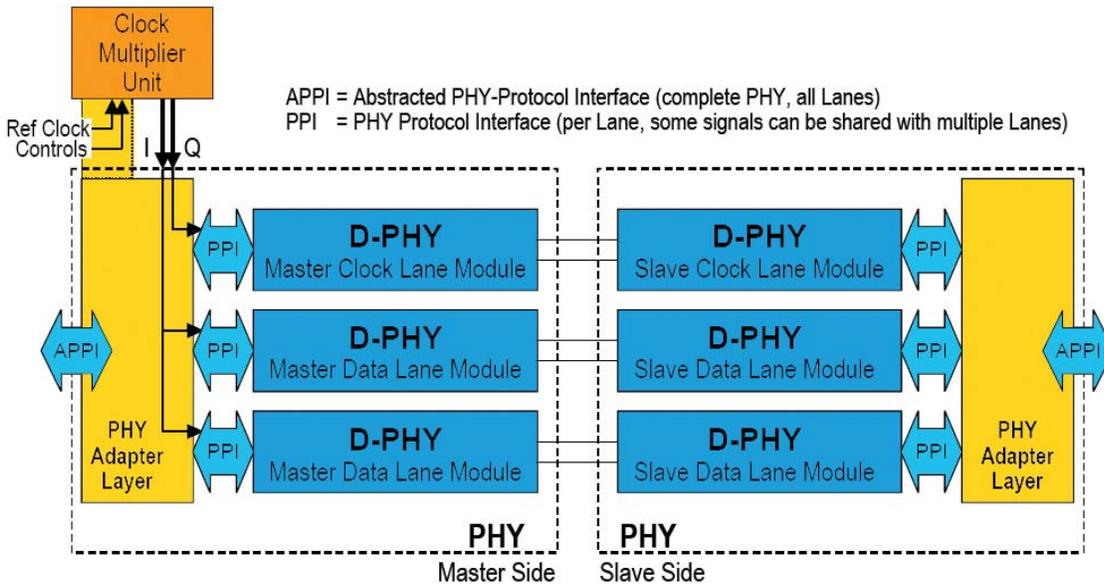

Figure 4: D-PHY Signaling Levels

Figure 5: Two Data Lane PHY Configuration

A complete link contains, beside lane modules, a PHY adapter layer that ties all lanes, the clock multiplier unit and the PHY protocol interface together. Figure 6 shows a PHY configuration example for a link with two data lanes plus a separate clock multiplier unit. The PHY adapter layer, connected via the logical PHY-Protocol interface (PPI) is not within the scope of this document. As shown in Figure 6, clock signals may be shared for all lanes.

A PHY configuration consists of one clock lane and one or more data lanes. All data lanes can support high-speed transmission and in the escape mode, forward direction.
There are two main types of data lanes:
• Bi-directional (featuring turnaround and some reverse communication functionality)
• Unidirectional (without turnaround or any kind of reverse communication functionality)
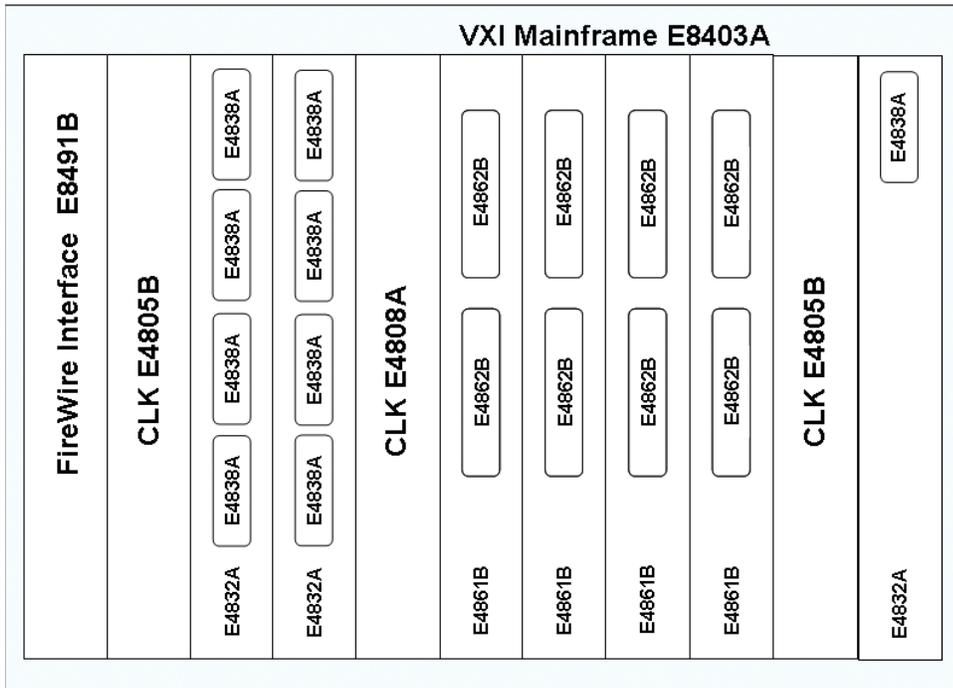
Figure 6: 81250A ParBERT configuration for testing a two lane phy configuration

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81250A ParBERT Configuration for Testing a Two Lane Phy Configuration

One low power lane consists of 2 x E4838A and one high speed lane consists of 2 X E4862B pattern generators, as shown in figure 8. In total a minimum of 2 data and 1 clock lane are required. The third clock-group is used as a clock source to synchronize the low and high speed clock groups, see figure 6.

For switching the transmitter from high speed differential to low power single ended mode, the HS TX has to be set into an idle mode, where both output will be at roughly the same "idle" level at VOLHB, see figure 4. Diving the idle correctly, creates the setup using two pattern generator channels. While on the complement output of the HS pattern generator the "idle" is the level zero or a logical 1, the "idle" on the normal output of the pattern generator is a level zero or the logical 0. This requires to set the normal output to "PAUSE0" and the complement output to "PAUSE1". For HS TX Mode, both pattern generator channels send the same pattern. The solution uses two data generator channels (E4861B data module and 2x E4862B 3.35G pattern generator front-ends) per data lane.

The normal and complement outputs are mixed with the LP pattern generator (E4832A data module and 2x E4838A 675M pattern generator per data lane) by using power dividers (2x 11636B). The wiring of one clock / data lane is shown in figure 7.

Figure 8 shows a picture of the wiring including the power dividers per lane. Included also is the recommended use of 500 ps transition time converters, which improve the signal integrity by reducing the ringing caused by reflections due to impedance mismatching.

For analysis an Agilent DSO8104A Infiniium scope is proposed, which allows to switch the input either to 1 MOhm in the LP TX mode or to 50 Ohm in the HS mode (actually using the E5380A SMA probe adapter head for the Infiniimax probe amplifier, which allows to measure just differential signals on one scope channel). With this analysis solution the termination is correct both for the LP and for the HS TX Mode. The scope does not switch between termination and un-terminated on the fly. For testing best strategy would be to force the MIPI TX in either LP or HS mode, but not with switching "on the fly". The Scope is only used for checking the signal levels and for calibration purposes. The ParBERT however can operate in both modes using the sequencer.
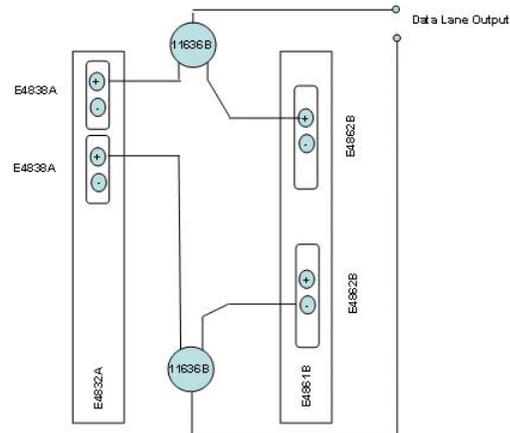
One low speed lane is 2 x E4838A   One high speed lane is 2 x E4862B

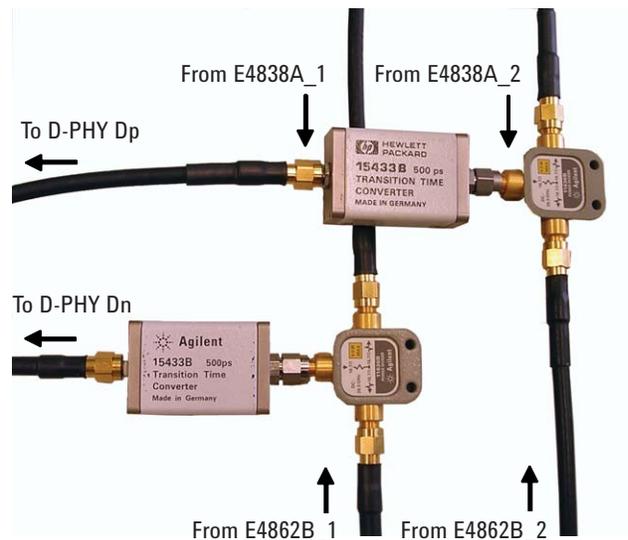Figure 7: Combining ParBERT channels to drive D-PHY clock/data lane

Figure 8: D-PHY Signal Conditioning

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Another issue is the jitter test. For the HS Tx the ParBERT pattern generators offer the capability of delay control inputs on each of the HS pattern generator. This allows the generation of jitter up to a jitter modulation frequency of 200 MHz and up to a jitter amplitude of 500 ps, which at 1 Gbps is equivalent to 0.5 UI. At the time of writting this document, the standard proposal did not include a procedure for RX test, but it would be a wise decision to make jitter tolerance tests during chip characterization.

Figures 9 to 11 show the signal switching between HS and LP mode obtained from a setup as described. Figures 11 and 12 zoom down to the bit level. As can be seen, the method of combination and switching provides clean and accurate signals.

Configuration information

Qty	P/N	Description
1	81250A	Parallel Bit Error Ratio Tester
1	81250A-148	13-slot VXI Mainframe
1	E4875A-ATO	ParBERT 81250 User Software.
1	81250A-013	IEEE 1394 PC link to VXI (Firewire)
2	E4805B-ATO	2.7 GHz Central Clock Module
1	E4808A-ATO	10.8 GHz High Performance Central Clock Module
3	E4832A-ATO	675 MHzModule
7	E4838A-FG	333kHz - 675 MHz Data Generator Front End
3	E4861B-ATO	3.35 Gbit/s Generator/Analyzer Module
6	E4862B-ATO	3.35 Gbit/s Generator Front End

For Analysis
	DSO8104A	Infiniium Oscilloscope
1	E5380A	SMA probe adapter head

Accessories
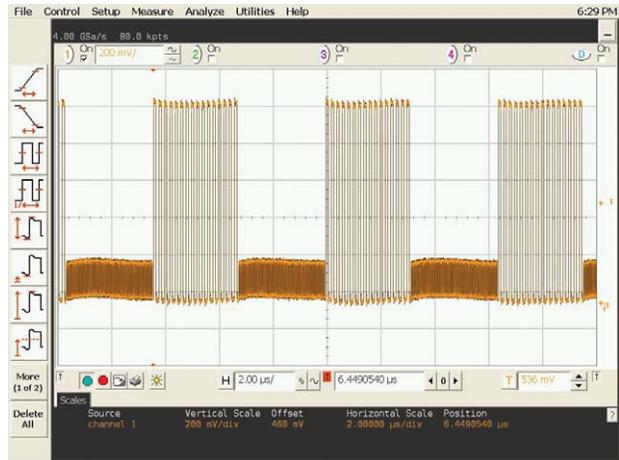|		
6	11636B	Power divider
6	15433B	Transition Time Converter
3	15442A	coaxial cables

Further cabling as required.

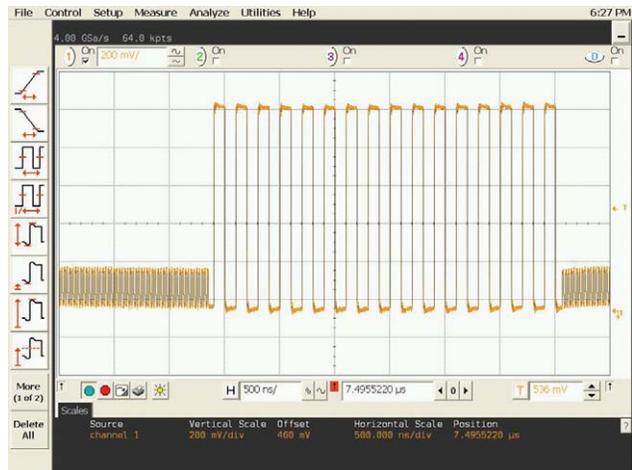Figure 9: the D-PHY stimulus signal switching between HS and LP mode

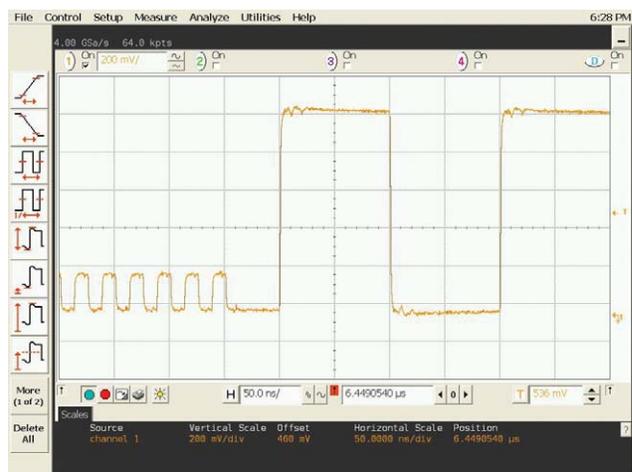Figure 10: Zoom into the D-PHY stimulus signal switching between HS and LP mode

Figure 11: Zoom into the bit level of the D-PHY stimulus signal switching between HS and LP mode

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Related Agilent Literature	Pub.No.
ParBERT 81250 Parallel Bit Error Ratio Tester Product Overview	5968-9188E
ParBERT 81250, Mux/Demux application Application Note	5968-9695E
Productivity Assistance	5980-2160E
Advanced Memory Buffer Application Note	5989-3481EN
ParBERT 81250 43.2/45 G Product Overview	5988-3020EN
ParBERT 81250 3.35G Optics Data Sheet	5988-5901EN
E4887A HDMI TMDS Signal Generator Data Sheet	5989-5537EN
Test Automation Software Platform N5990A Data Sheet	5989-5483EN

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