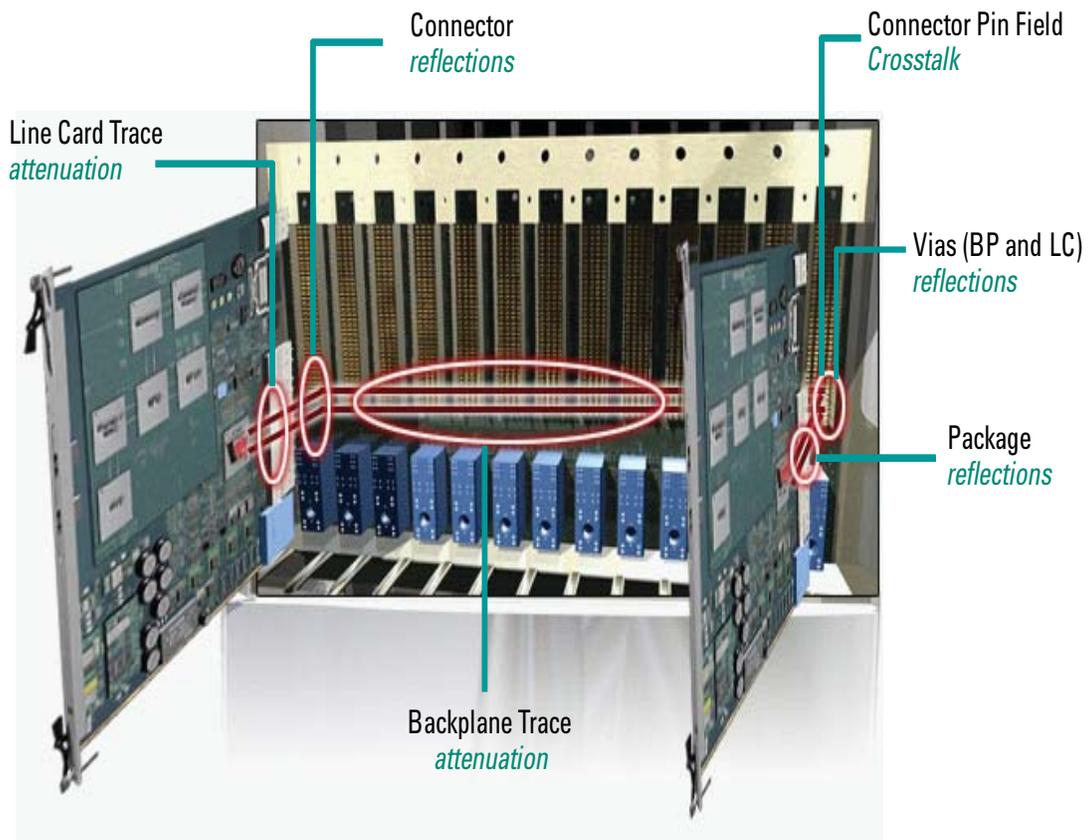
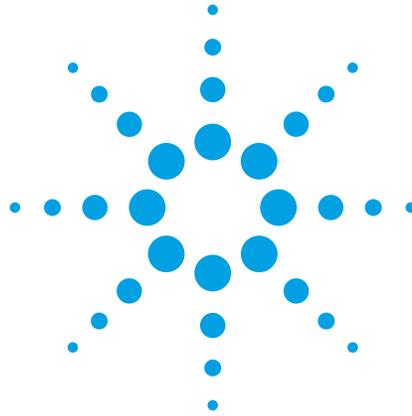


A Design of Experiments for Gigabit Serial Backplane Channels

Application Note



Introduction

Tomorrow's generation of consumer products will exploit the triple play of telecommunication – voice, video, and data. This new development will merge two broadband services, high-speed Internet access and television with one narrowband service over a narrow band service such as telephone. In order to support the extraordinary amount of bandwidth required by this broadband service, the internet infrastructure is transforming into a superhighway of information. High-speed internet switch and router equipment performance is a critical component that will dictate the outer limits of this network. The high-speed backplane within the aforementioned network equipment is the fundamental backbone of this physical layer that will sustain future technologies of advanced line cards containing ultra-fast serializer-deserializer chipsets.

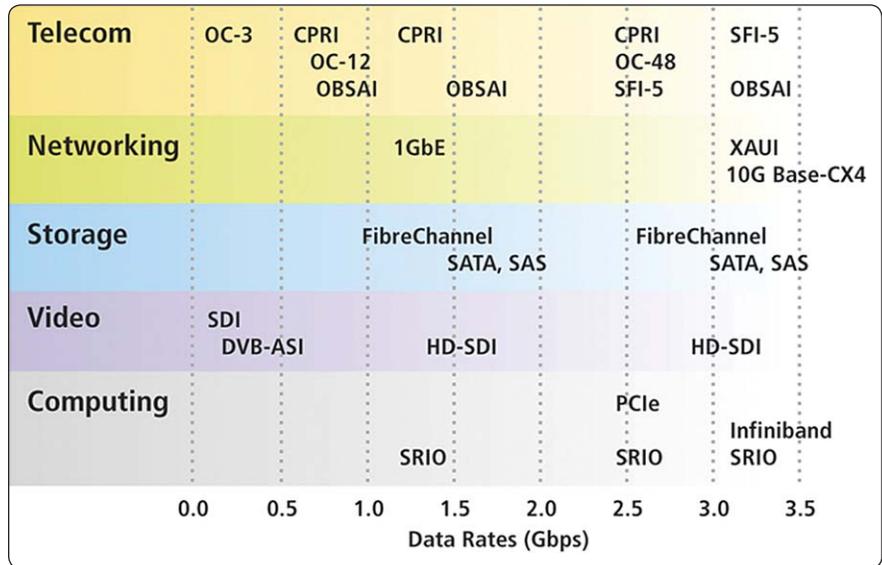


Figure 1. Serial Standards

This market demands that backplanes provide more bandwidth than ever. The answer for this demand is backplanes with many multi-gigabit serial channels. Designing, building, and characterizing these backplanes are becoming more challenging with every increase in the serial bit rate. A network equipment manufacturing company's whole product line depends on the longevity of the backplane. Upgrade and innovation are implemented with daughter cards, but the backplane is the anchor that holds the customer base. Because of this, backplanes have to be designed and built to last often through several line card product generations. Although the backplane usually has no active components, a significant effort must be expended to characterize and verify its performance. There are 3 commonly used tools for characterizing multi-gigabit interconnects, the TDR, the VNA, and the Eye diagram.

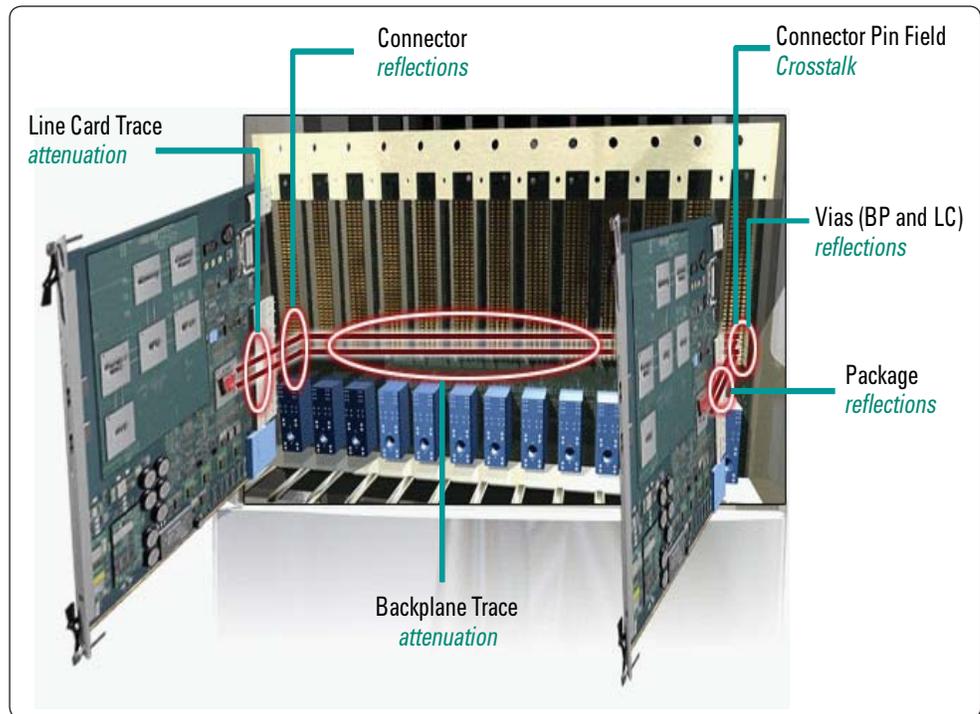


Figure 2. The Serial I/O Channel

Serial Backplane Channels

Any backplane based system is composed of the same basic components, the line/daughter cards and the backplane. The signal path for communication between 2 daughter cards over a backplane channel consists of a number of transitions. Starting with the transmitter die, the signal path includes transitions from the transmitter die to the package, to the printed circuit board transmission line, to the backplane connector, to the backplane transmission line, to the far end daughter card backplane connector, to the daughter card transmission line, to the package and finally to the die at the receiver. Each of these transitions is an opportunity for the signal to be degraded.

The transitions result in degradation as a result of reflections, attenuation, and interference. At the connector pin field impedance mismatch results in reflections that add to the jitter in the signal at the receiver. Likewise, attenuation in the signal from the transmission line further increases the jitter by generating inter-symbol interference. In addition, signals on other channels can induce crosstalk noise in the signal path and thereby increase even further the eye closer at the receiver. Since all of these can work together to reduce the quality of the signal at the receiver, we must characterize the backplane channels to insure acceptable performance for the application.

Backplane Platform Description

At Xilinx, they have built a backplane that would be a platform for demonstrating the usage and operation of the Xilinx Virtex-5 GTP Multi-gigabit Transceivers in a backplane application. The demonstration backplane provides a variety of channel behaviors. These behaviors are the result of a number of variations in materials, components, and routing structures. The demonstration backplane also has structures that allow for some decomposition of the channel path. With these structures, the root cause of some channel responses can be isolated.

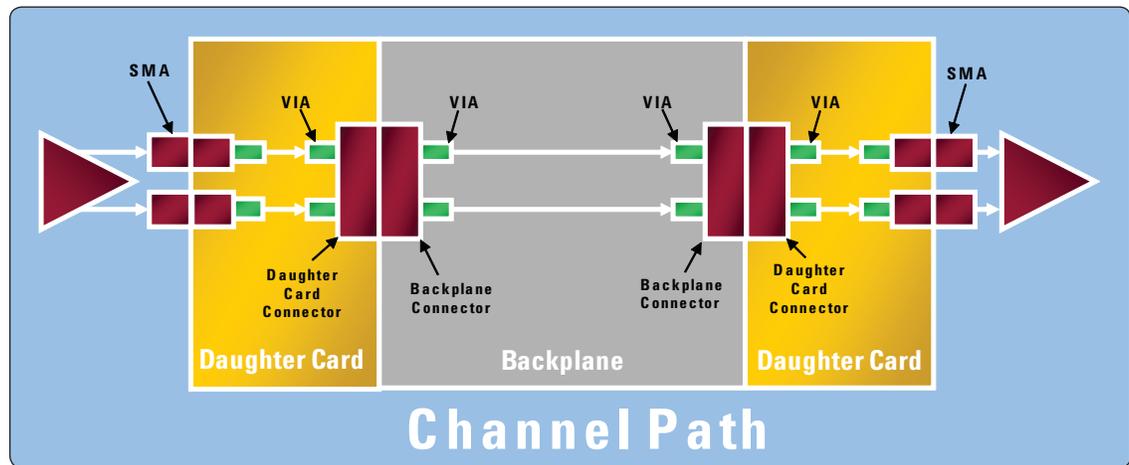


Figure 3. Platform Channel Path

This demonstration platform consists of a backplane board and daughter card boards. On the daughter card, the channel path, as shown in Figure 3, starts with an SMA launch into the daughter card, then propagates through a transmission line from the SMA to the backplane mating connector. On the backplane, the channel path runs from one backplane connector through a transmission line to another backplane connector that mates with the destination daughter card. By varying the connector type, the printed circuit board dielectric material, the routing length and routing layer, the backplane and daughter cards can provide a variety of channel behaviors.

In addition, to the standard channel path, the demonstration backplane has reference channels. These channels provide a means to decompose the channel path and give visibility to some intermediate channel path structures. The demonstration backplane actually consists of a number of experiments that involve variations in PCB dielectric materials, backplane connectors, channel length, channel physical structure and channel physical path routing.

There are three connector types on the backplane. The connectors were selected to cover a range of backplane channels that an engineer may encounter when designing for a multi-gigabit transceiver. To represent a legacy channel, the HM 2mm connector was selected. With the advent of Advance TCA backplanes, the HM-Zd connector was selected to represent a popular contemporary serial backplane channel. The Amphenol eHSD connector was selected to represent a higher performance channel.

Table 1. Dielectric Material Properties

Material	Dielectric Constant	Loss Tangent
Nelco 4000-13	3.7	0.009
Nelco 4000-13si	3.4	0.008
ISOLA FR408	3.7	0.012

Notes

1. 50 percent resin content
2. Test frequency is 1 GHz

The backplane was built using three types of dielectric material, ISOLA FR408, Nelco 4000-13 and Nelco 4000-13si. Although all of the materials are upgrades to standard FR-4, they do provide variation in performance as is shown in Table 1. The values in this table were obtained from the manufacturer’s published product brochures.

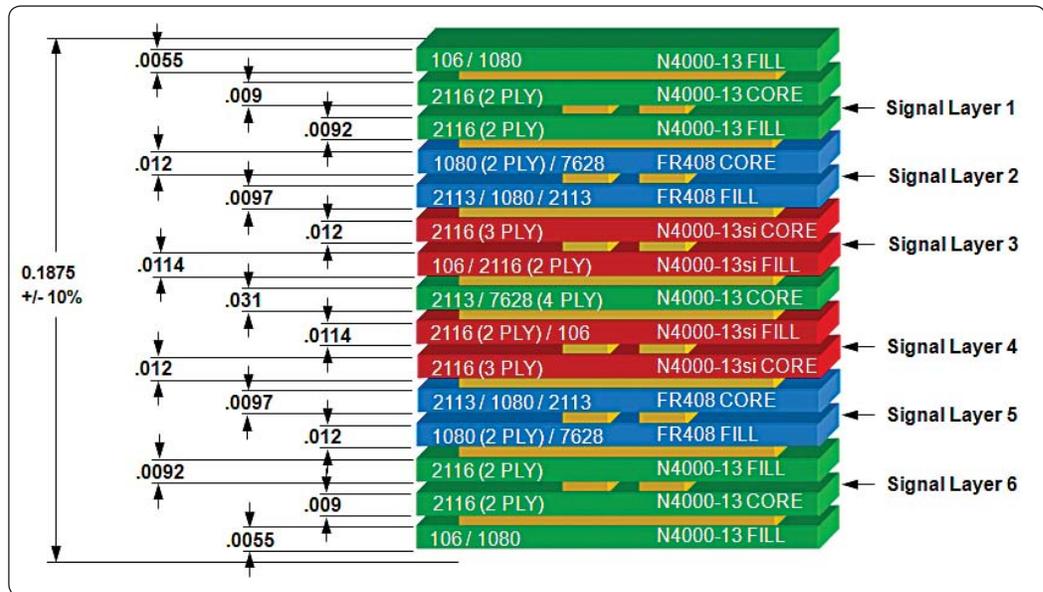


Figure 4. Backplane Stack-up

The backplane stack-up consists of six signal layers and eight internal plane layers for a total of 16 layers. With the cooperation of Sanmina-SCI, a single stack-up was designed that included all of the dielectric material types. As shown in Figure 4, the stack-up was designed so that each material type is represented by two routing layers, one in the upper half of the stack-up and another place symmetrically in the lower portion of the stack-up. As we will see, besides allowing for manufacturing issues, having the opposing pairs of routing layers for each of the board material types adds variation to channel performance. As also shown, the overall thickness of the backplane is 187 mils.

Backplane Platform Description (cont'd.)

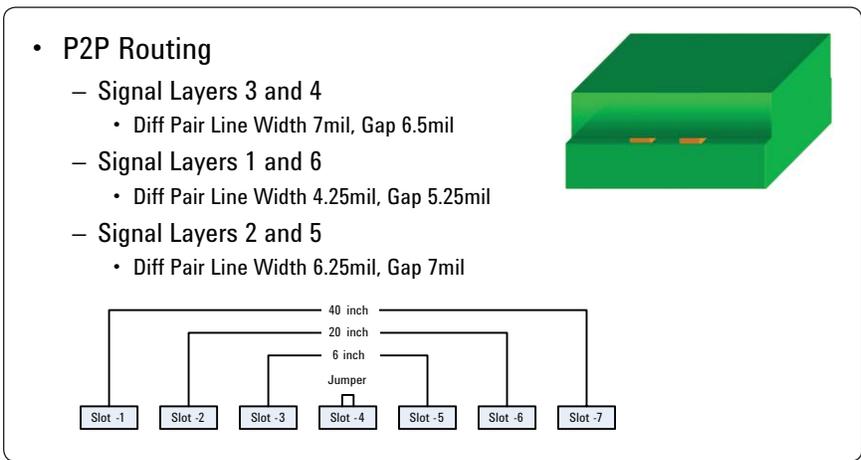


Figure 5. Backplane Trace Geometry

The backplane has four lengths of point-to-point channels on each of the connectors. The shortest length is actually a jumper from one set of pins on a backplane connector to another set of pins. This path virtually eliminates signal degradation due to transmission line attenuation in the backplane. The other lengths are 6, 20, and 40 inches. The trace geometries for each of the layers are also shown in Figure 5.

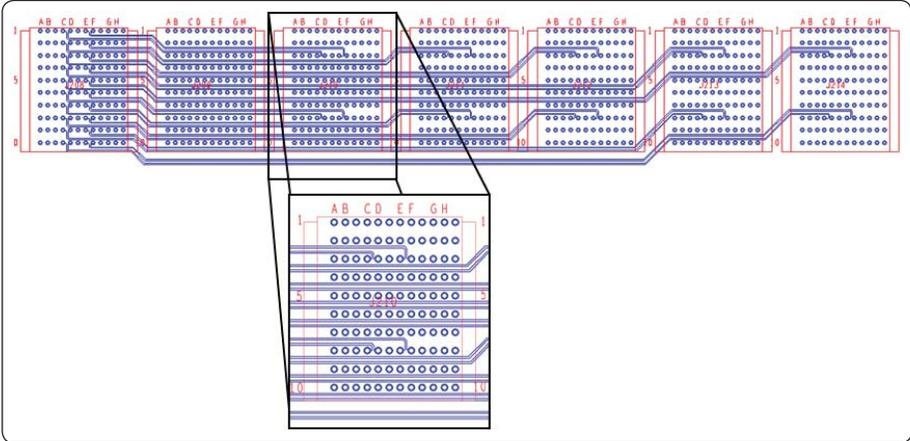


Figure 6. HM-Zd Routing

As there are many combinations of trace geometry and layer thickness, it should be noted that for layers 1 and 6, the trace geometry was driven by the desire to implement the quad-route routing as recommended by Tyco for HM-Zd connectors. This routing technique offers a greater signal density in the backplane because it doubles the number of traces that can be routed on each layer between the HM-Zd pin rows.

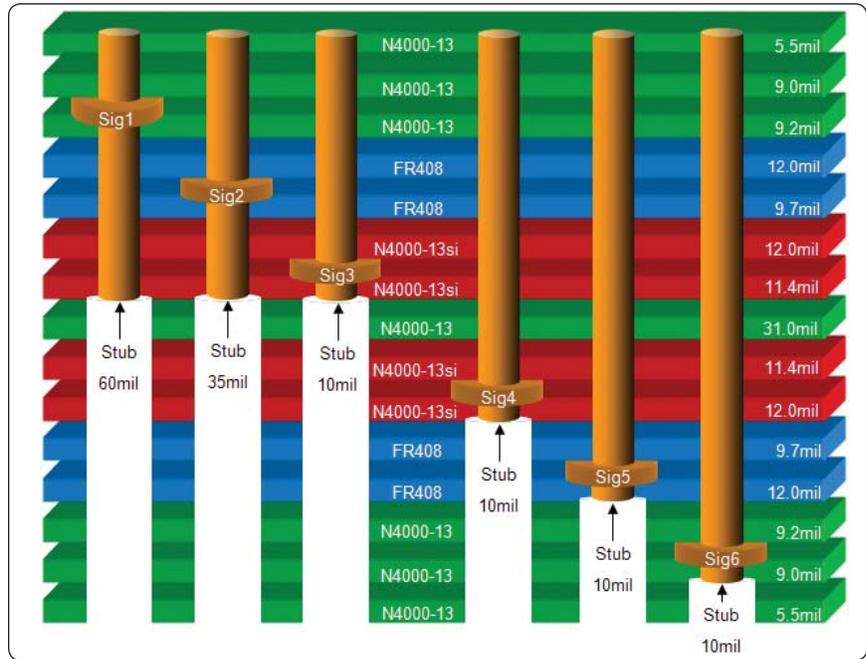


Figure 7. Backplane Via Stubs

Under normal circumstances a backplane must be built with enough mechanical strength to support the stresses of insertion and removal of daughter cards. Because of this, and the need to have a significant number of signal routing layers, the backplane is usually thicker than most other types of circuit boards. For this reason, we built the demonstration backplane with an overall thickness of 187 mils.

Because of the backplane board thickness, channels routed on the upper layers exhibit a significant via stub length. These via stubs can be a source of channel signal degradation because of the reflections generated by the stub. A widely accepted practice to minimize the affects of via stubs is to backdrill the vias to eliminate the stub. The board fabricator, in this case Sanmina-SCI, is able to backdrill a via to within 10 mils of the signal layer.

Therefore, the specified backdrill depth for each of the layers was calculated based on this requirement. That is except for signal layers 1 and 2. Because press-fit compliant pin connectors were used on the backplane, the upper 2 layers could not be back-drilled to within 10 mils of the signal layer. The compliant pins require a minimum via barrel depth of 62 mils. Therefore, the vias for signals routed on these layers could only be backdrilled to within 72 mils of the top of the board. As shown in the figure, this means that channels routed on the upper layers still had some via stubs. The affects of these stubs on channel performance is included in the characterization.

In addition to the normal channel paths from slot to slot, the backplane also has a series of reference channels. There are 6 reference channels on the backplane, one for each of the signal layers. Each reference channel uses SMA connectors for launching and retrieving signals. The reference channels are routed as balanced signal paths using the same trace geometry as that of the other traces on the layer and have a trace length of 20 inches. The SMA connectors are compliant pin press-fit connectors. By removing the daughter card and backplane connectors from the channel path, the reference channel provides for a more simplified signal path on the backplane, and allows visibility into the behavior of the backplane transmission lines on each layer.

Daughter Card Description

In addition to the backplane, the demonstration platform includes daughter cards. These cards use SMA connectors to launch signals into and retrieve signals from the backplane. For each of the connector types, the daughter card has a number of channels. For the eHSD connector, the daughter card has 24 channels. For the HM-Zd connector, there are 32 channels and for the HM 2mm connector there are 16 channels. The trace length for all connections between the SMA connectors and the backplane connector pins is eight inches. All of the channels are routed as balance pairs. There are also four reference channels that are routed as single ended connections between two SMA connectors on the daughter card.

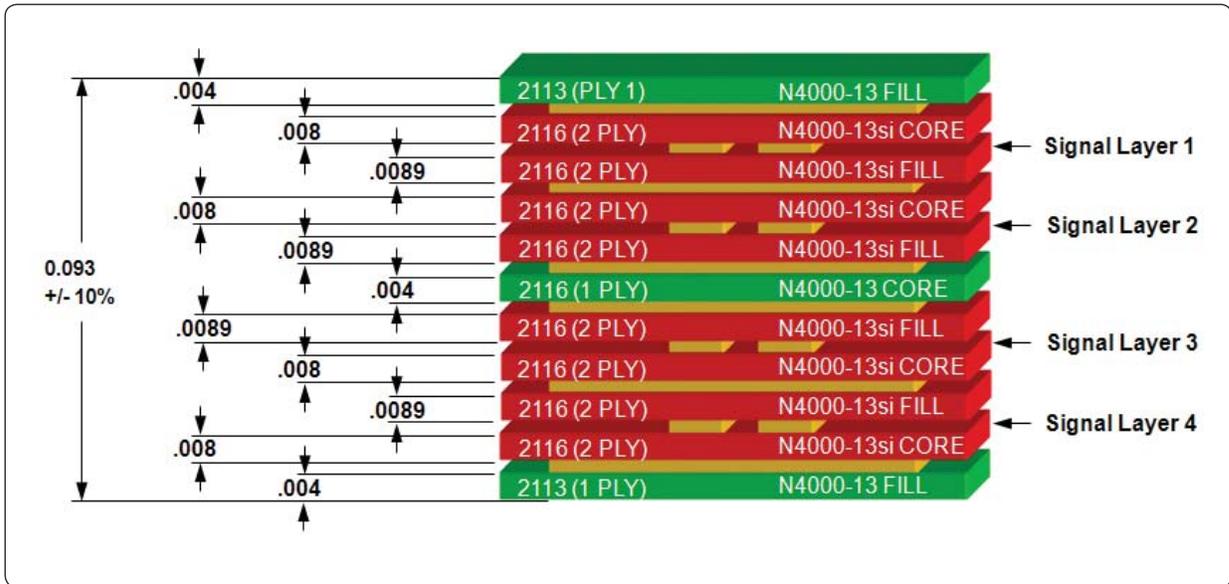


Figure 8. Daughter Card Stack-up

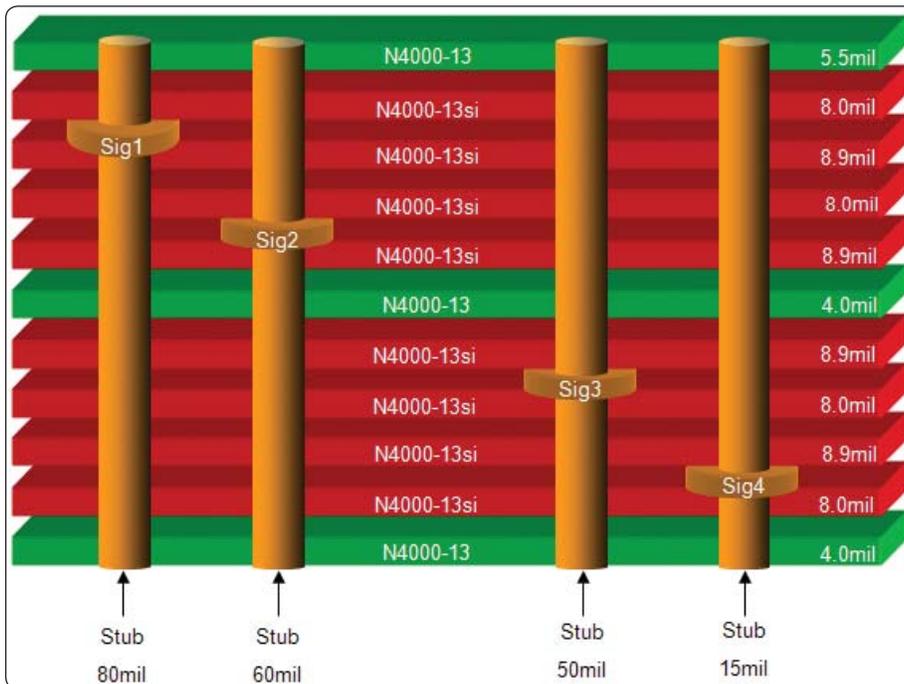


Figure 9. Daughter Card Via Stubs

The stack-up for the daughter card has four signal layers, and six internal plane layers for a total of 12 layers. Signals are not routed on the top and bottom layers. The daughter card uses Nelco 4000-13si as the dielectric material around all of the signal layers. Since this is the highest performing material that we used on the backplane, we chose it for the daughter card in order to limit the attenuation in the daughter card signal path. The overall thickness of the daughter card is 93 mils, a common daughter card thickness.

As in the case of the backplane, the routing layers that are closer to the top of the board have longer via stubs. With the effects associated with varying stub lengths on the daughter card, the demonstration platform is able to provide a variety of channel behaviors.

Backplane Characterization

The performance of the demonstration platform was characterized and verified using a combination of time domain and frequency domain test and analysis. The insertion-loss for the channels was evaluated for performance over the band of interest.

As with any product, the development effort must be bounded by a set performance requirements. Because backplanes are usually required to be usable over several product performance upgrades, it must be designed to meet the immediate and future performance demands of the product. To emulate such a product development, the demonstration platform was characterized for an immediate requirement of 3.125 Gb/s and a future requirement of 6.25 Gb/s.

For the demonstration platform, each of the channel types was tested and analyzed over the required ranges of performance. The analysis includes insertion loss, TDR, and eye diagram analysis. The insertion loss data provides a view of the overall frequency response of the channel. Combining insertion loss with TDR data gives a more complete picture of the performance of the channel by providing information on the effects of each transition in the channel path on the overall response of the channel. Eye diagram analysis using data collected from the VNA was performed to acquire an understanding of the effects of attenuation, and reflection on the performance of each channel.

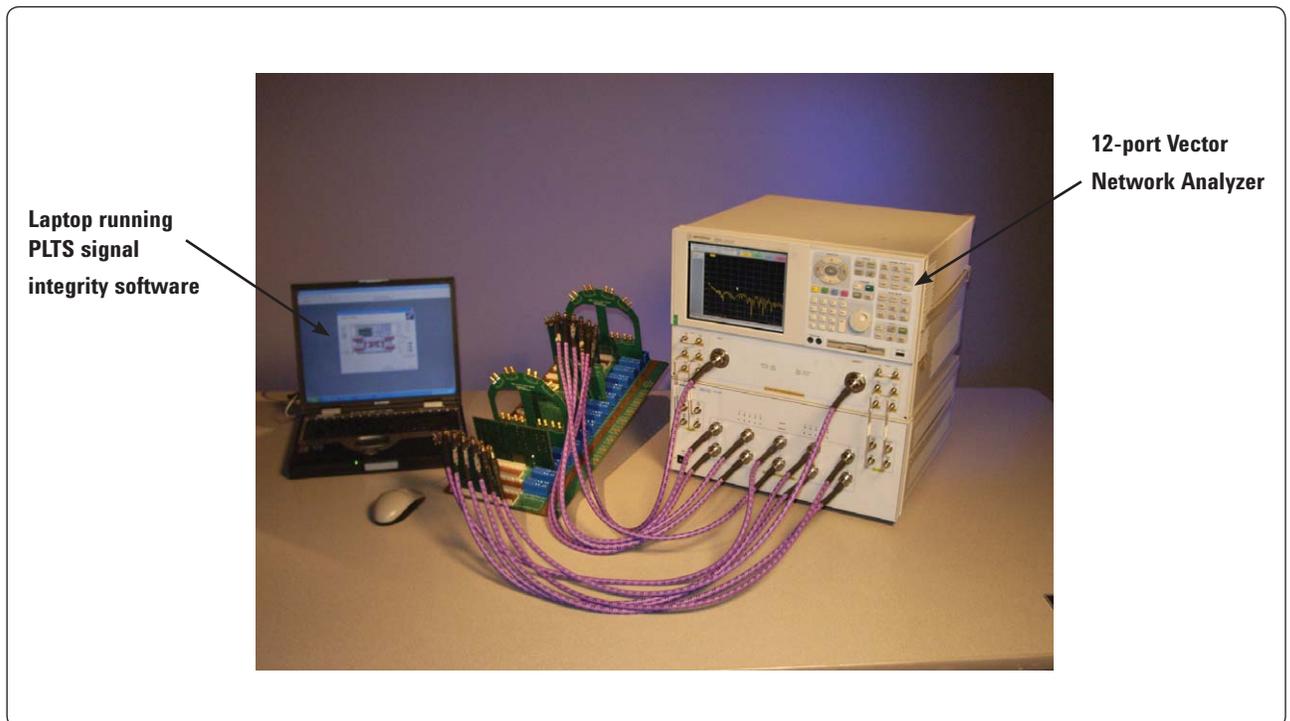


Figure 10. Test Setup

The test set-up for this design of experiments was a 12-port vector network analyzer (VNA) controlled by a laptop running Physical Layer Test System (PLTS) signal integrity software. The resultant data files were a Touchstone format s-parameter file with an *.s12p suffix. This is a standardized file format used frequently in the modeling and simulation industry that allows import and export into many different design tools. Advanced Design System (ADS) is one popular tool that is starting to migrate from the microwave industry to the high-speed digital industry. In any case, the PLTS system was used to gather differential data in all domains of analysis, including frequency, time, eye diagram and RLCG modeling. The most pertinent data obtained from PLTS was used to quickly optimize the design of this backplane and will be shown in this paper.

Backplane Characterization (cont'd.)

The channel performance was evaluated by connector type and by channel path. For each of the connector types there are a number of channel paths. These channel paths vary by layer on the daughter card, and on the backplane. All the tests were performed on the channels with 20 inches of backplane trace length. To aid in managing the testing, a matrix was developed for each connector type. This matrix shows the path of each channel on the daughter card and on the backplane.

Table 2. eHSD Channel Path Matrix

					Backplane					
					Sig1	Sig2	Sig3	Sig4	Sig5	Sig6
					4000-13	FR408	4000-13si	4000-13si	FR408	4000-13
					A-B	A-B	A-B	C-D	C-D	C-D
					9-12	5-8	13-16	13-16	5-8	9-12
Line Card	Sig	Diff Pair	Row	Pins						
Line Card	Sig1	105-108	A-B	13-16			4000-13si			
		121-124	A-B	5-8		FR408				
	Sig2	113-116	A-B	9-12	4000-13					
	Sig3	109-112	D-C	9-12						4000-13
	Sig4	101-104	D-C	13-16				4000-13si		
		117-120	D-C	5-8					FR408	

eHSD Connector Channels

Table 2 is the path matrix for the Amphenol eHSD connector channels. Each channel on the daughter card is identified by a differential pair number. The channels are routed in groups of four channels for each channel path type. On the daughter card, there are four signal layers. Each of the signal paths on the daughter card are routed to a signal layer on the backplane.

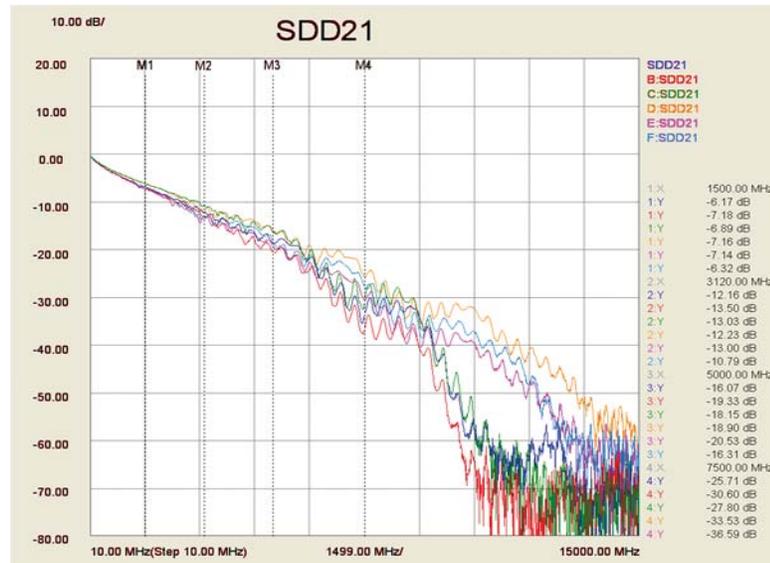


Figure 11. eHSD Channel Insertion Loss

The insertion loss data for the Amphenol eHSD channels is in Figure 11. The channel behavior tends to fall into one of two groups. As would be expected, the channels that are routed on the upper layers of the daughter card and backplane have lower operating bandwidth than do the channels that are routed on the lower layers. We attribute this behavior to the effects of the via stubs on signal integrity.



Figure 12. eHSD Channel TDR

With the TDR data, the impedance discontinuities are greater for the daughter card SMA launch than for the backplane connectors. Also, the magnitude of the impedance discontinuities is relative to the amount of stub length.

Table 3. HM-Zd Channel Path Matrix

				Backplane							
				Sig1	Sig2	Sig3	Sig4	Sig5	Sig6		
				4000-13	FR408	4000-13si	4000-13si	FR408	4000-13		
		Diff Pair	Row	C-D	E-F	A-B	A-B	G-H	G-H	C-D	E-F
			Pins	2-5	2-5	6-9	2-5	2-5	6-9	6-9	6-9
Line Card	Sig1	205-208	A-B	2-5			4000-13si				
		221-224	A-B	6-9		FR408					
	Sig2	209-212	C-D	2-5	4000-13						
		225-228	C-D	6-9						4000-13	
	Sig3	213-216	E-F	2-5		4000-13					
		229-232	E-F	6-9							4000-13
	Sig4	201-204	G-H	2-5				4000-13si			
		217-220	G-H	6-9					FR408		

HM-Zd Channels

Table 3 shows the path matrix for the HM-Zd connector channels. It should be noted that the channels routed on backplane signal layers 1 and 6 are routed using the Tyco recommended Quad-Route method.

HM-Zd Channels (cont'd.)

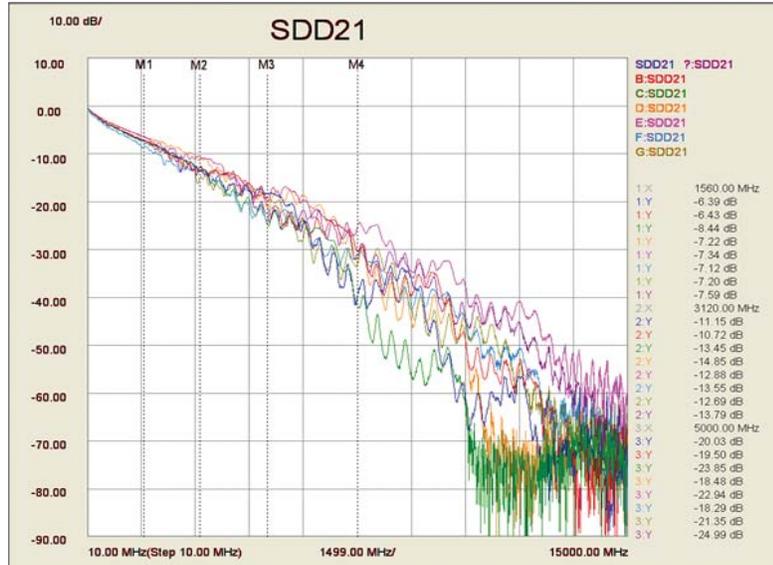


Figure 13. HM-Zd Channel Insertion Loss

Figure 13 shows the insertion loss for the HM-Zd channels. The traces on the plot are labeled to show the daughter card and backplane signal layers that were used to route the signal. So as in the case of second label, Sig3/Sig1, the path is from signal layers 3 of the source daughter card to signal layers 1 of the backplane to signal layers 3 of the destination daughter card.

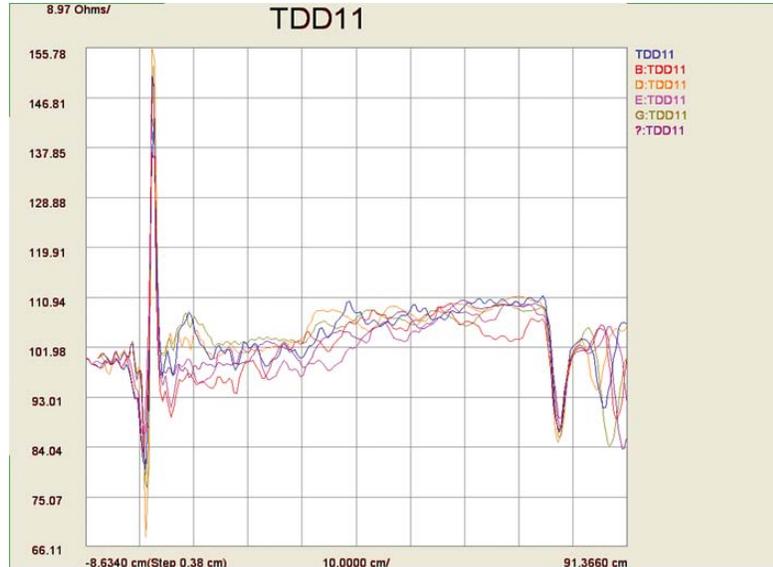


Figure 14. HM-Zd Channel TDR

The TDR data for the HM-Zd channels shows that the SMA launch on the daughter card has a greater impedance discontinuity than does the backplane connector interface.

HM-2mm Channels

Table 4 shows the path matrix for the HM-2mm connector channels. As previously mentioned, the HM-2mm connector channels are designed to represent a legacy backplane. For this reason, back-drilling was not specified for any of the channels on the HM-2mm connector. The signal pin assignment includes a liberal use of ground pins. Channel signal and differential signal pairs are grouped by two's with ground connections assigned to all of the connector pins that are adjacent to them.

Table 4. HM-2mm Channel Path Matrix

				Backplane																	
				Sig2				Sig3				Sig4				Sig5					
				FR408				4000-13si				4000-13si				FR408					
				A-B				A-B				D-E				D-E					
		Diff Pair	Row	Pins	11	12	14	15	2	3	5	6	2	3	5	6	11	12	14	15	
Line Card	Sig1		307	A-B	3						13si										
			305	A-B	6								13si								
			314	A-B	12		408														
			316	A-B	15				408												
	Sig2		308	A-B	2					13si											
			306	A-B	5							13si									
			313	A-B	11	408															
	Sig3		315	A-B	14		408														
			304	D-E	2								13si								
			302	D-E	5										13si						
			309	D-E	11													408			
	Sig4		311	D-E	14															408	
			303	D-E	3										13si						
			301	D-E	6											13si					
			310	D-E	12														408		
		312	D-E	15																408	

The insertion loss data for the HM-2mm channels are shown in Figure 15. Once again, we see from the data that the channels that are routed on the upper layers of the daughter card and the backplane have a lower channel bandwidth than do the channels that are routed on the lower layers. Because of the lack of back-drilling on these vias, the channel bandwidth is even lower than that of the other two connector types.

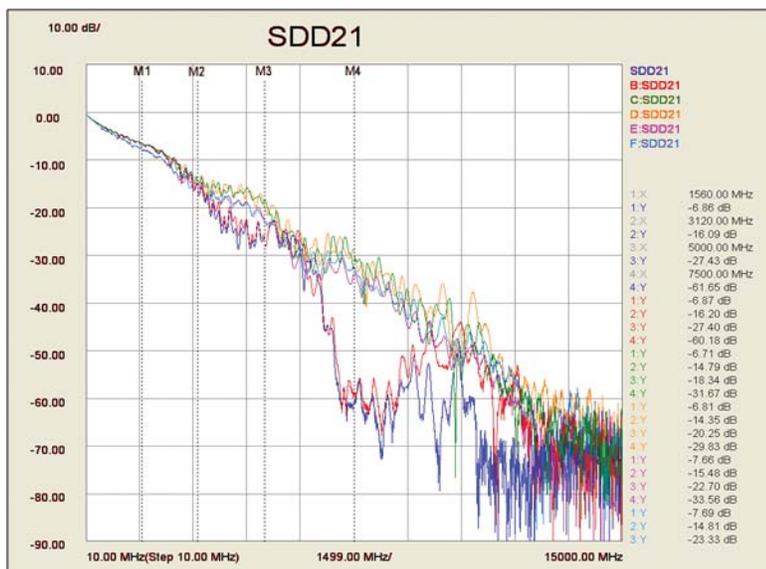


Figure 15. HM-2mm Channel Insertion Loss

HM-2mm Channels (cont'd.)

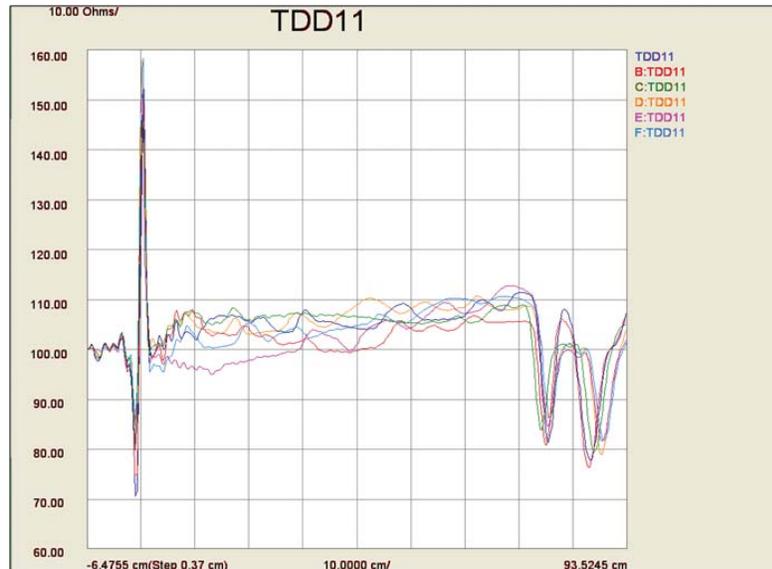


Figure 16. HM-2mm Channel Insertion Loss

The TDR data for the HM-2mm connector reveals the same large discontinuity in the SMA launch on the daughter card. It also shows a larger impedance discontinuity at the backplane connector interface.

Crosstalk Measurements

The channel to channel crosstalk will now be investigated for each of the connector types using a 12-port VNA. We set up each test to evaluate the crosstalk from two aggressor channels on a single victim channel. We tested the crosstalk affects based on the physical location in the connector of the victim channel pins relative to the location of the aggressor channel pin.

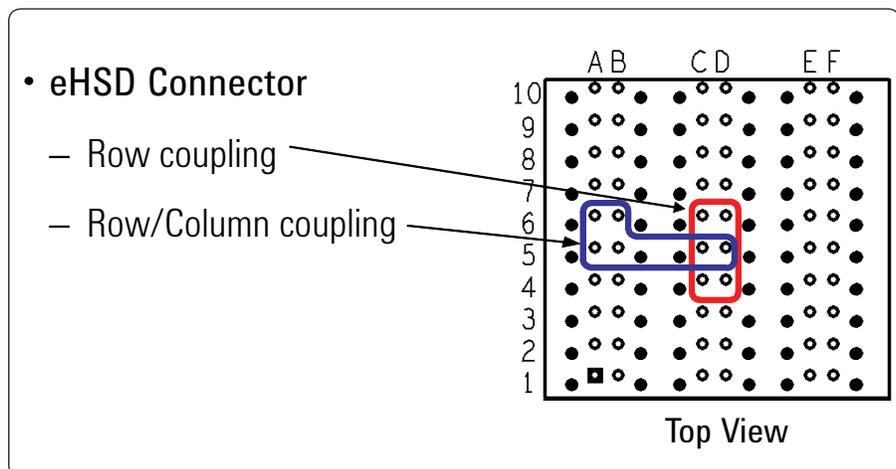


Figure 17. eHSD Crosstalk Configurations

For the eHSD connector, we tested the row coupling and row/column coupling as shown in Figure 17.

Observing the time domain differential (TDD) data for the near end crosstalk between the aggressor channels to the victim channel, reveals an area of significant crosstalk relative to other portions of the channel. By temporally marking the crosstalk region on the time domain near-end crosstalk TDD, the location of the vertical marker in the differential time domain reflection of the victim channel, TDD33 shows the channel structures that are contributing to the crosstalk (because the waveforms in Figures 18 and 19 are “time-aligned” sharing the same horizontal timebase). In this case, the pin field via for the backplane connector is the major contributor. It should be noted that the temporal plot shows that the contribution to crosstalk is primarily from the pin field vias and not the connector itself.

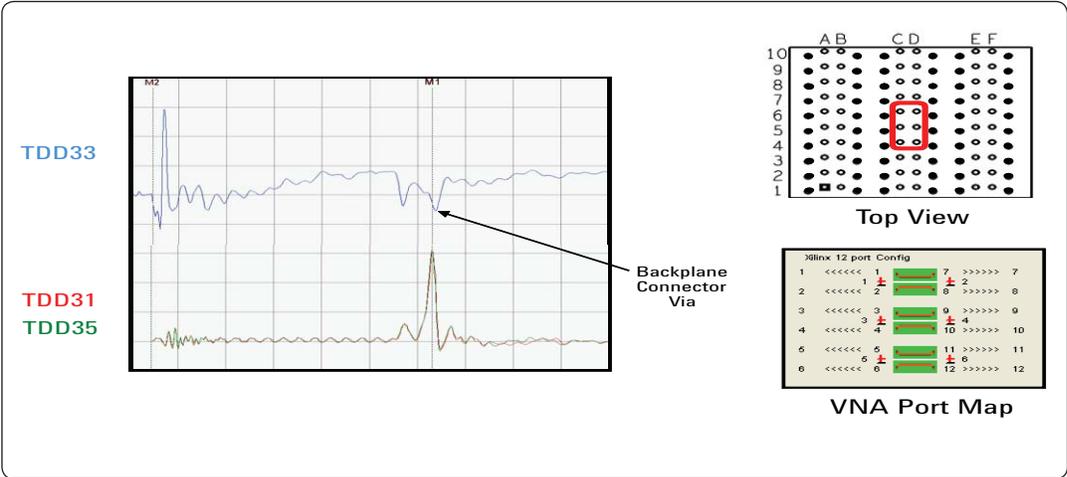


Figure 18. eHSD Channel Row Crosstalk

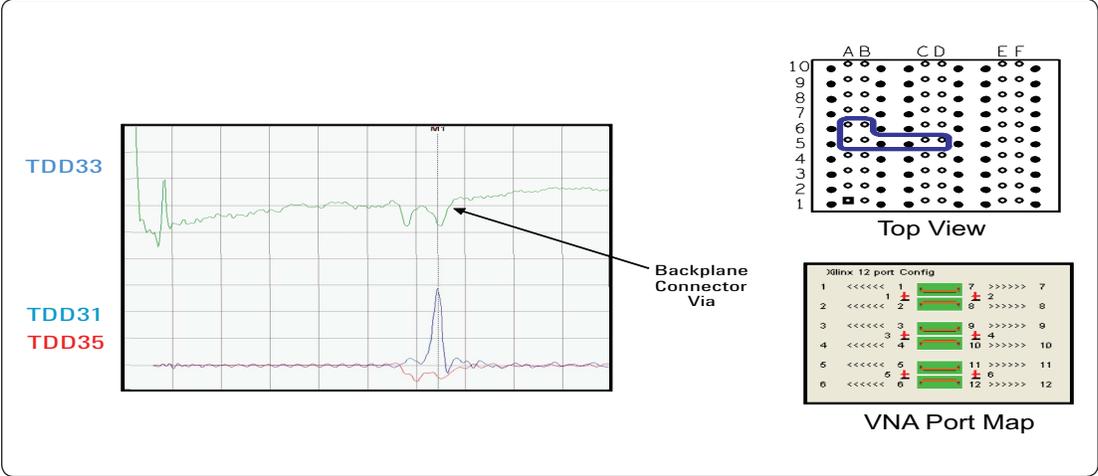


Figure 19. eHSD Channel Row/Col Crosstalk

The same measurements were performed for near-end crosstalk for row/column channel pin pair patterns, as shown in Figure 19. As expected, the row coupling in this test was the same as was measured for the previous row coupling test. Intuitively, the column coupling magnitude should be less than that of the row coupling due to the addition of ground pins between the two differential channels. The data reveals that this is the case.

Crosstalk Measurements (cont'd.)

The HM-Zd connector was tested for near-end crosstalk in both a row and column configuration.

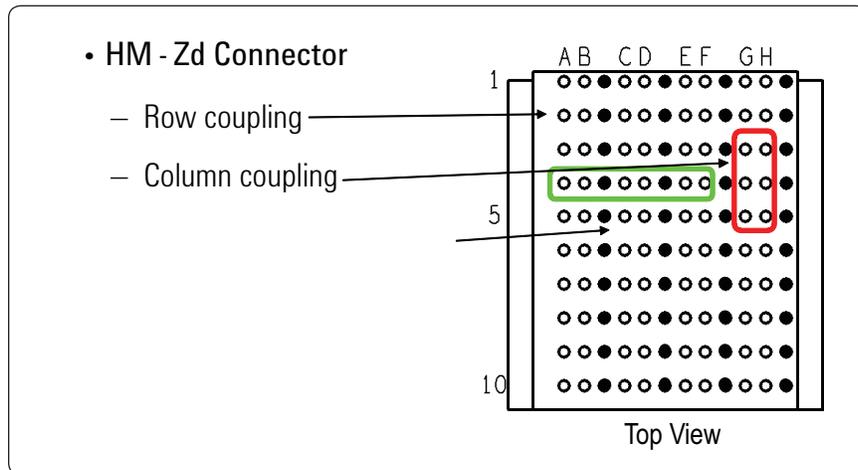


Figure 20. HM-Zd Crosstalk Configurations

The HM-Zd connector was tested for near-end crosstalk in both a row and column configuration.

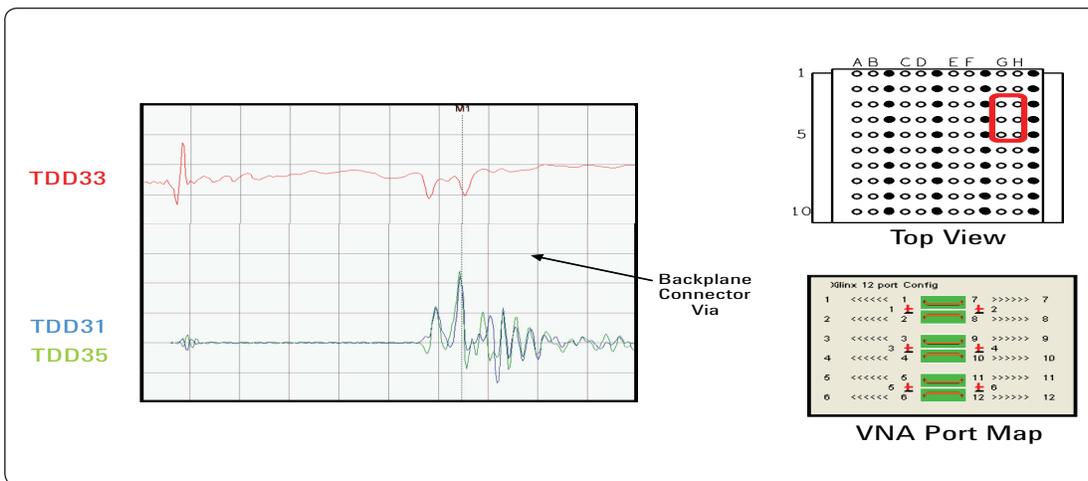


Figure 21. HM-Zd Channel Row Crosstalk

The data from the row coupling tests shows that the major contributor is once again the connector pin via field on the backplane.

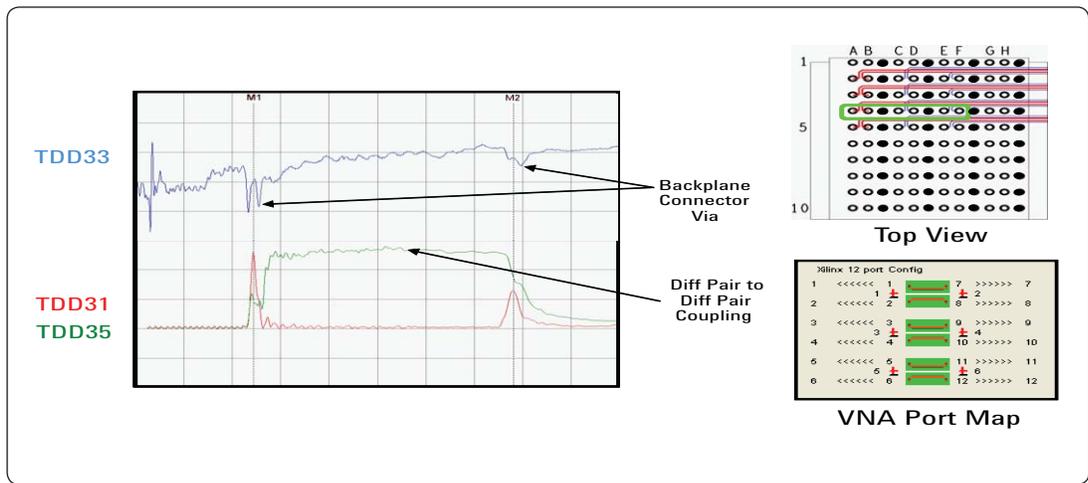


Figure 22. HM-Zd Channel Column Crosstalk

The column coupling tests gave some interesting results. For the row coupling case, the crosstalk results were similar to those of the previous test that tested only row coupling. This was not a surprise. The column channel arrangement gave a unique near-end crosstalk result. As can be seen in the figure, a significant amount of the crosstalk between the two channels occurred in the backplane traces.

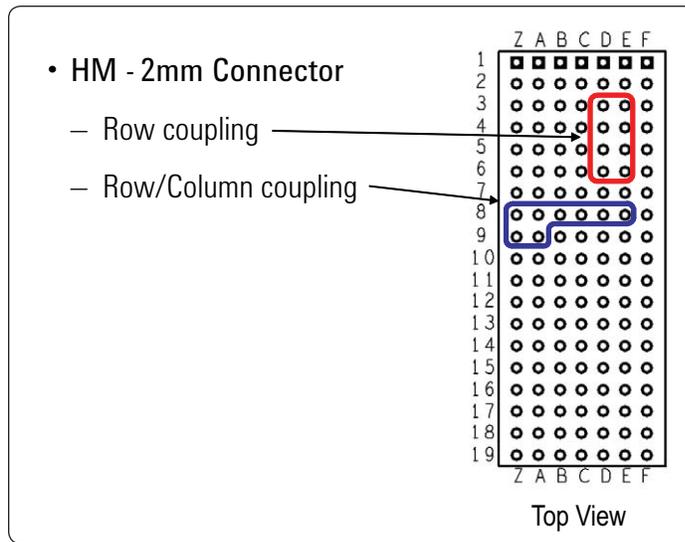


Figure 23. HM-2mm Crosstalk Configurations

Pins were assigned on the HM-2mm connectors so that rows of pins are separated by rows of ground pins. The usage of ground pins in this manner is not an uncommon practice for these types of connectors.

Crosstalk Measurements (cont'd.)

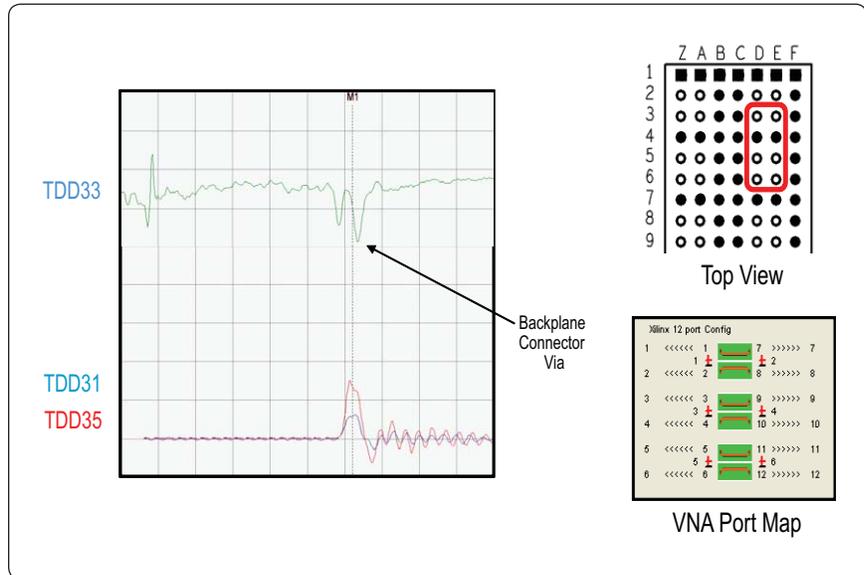


Figure 24. HM-2mm Channel Row Crosstalk

The near-end crosstalk test data shows that unlike the other two types of connectors, the major portion of the coupling is in the HM 2mm connector. As can be seen in the TDD33 plot in Figure 24, the crosstalk peak appears between the backplane connector vias on the daughter card and on the backplane. Also notice there is less crosstalk from the aggressor channel that is separated from the victim by a set of ground pins.

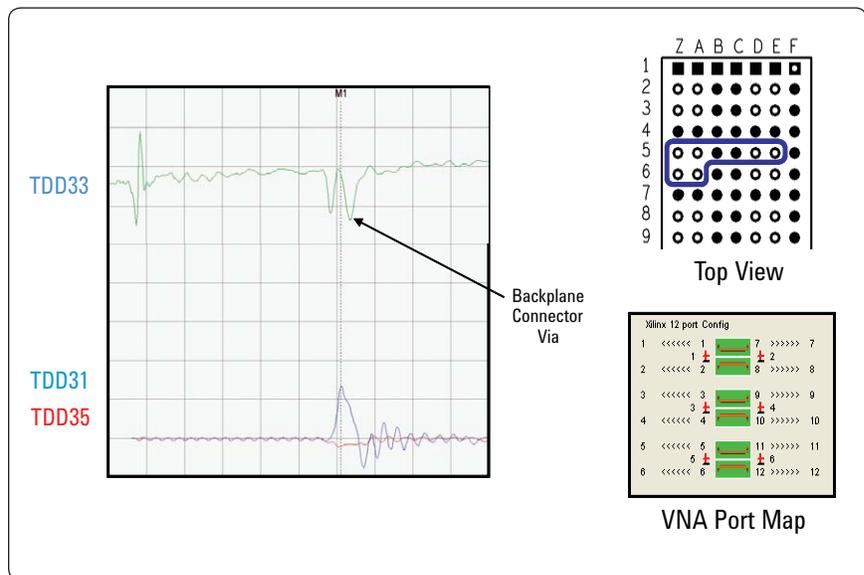


Figure 25. HM-2mm Channel Row/Col Crosstalk

For the row/column tests the HM-2mm shows crosstalk coupling in the connector for the row coupling portion. For the column coupling the amount of crosstalk coupling is substantially less than the row crosstalk coupling.

Eye Diagram Analysis

After evaluating the channels for specific parametric responses, they were analyzed using the collected channel measurements to perform an eye diagram analysis. This analysis provides a method to qualitatively evaluate the overall performance of the channel. As in the previous tests, the channels were analyzed by connector type.

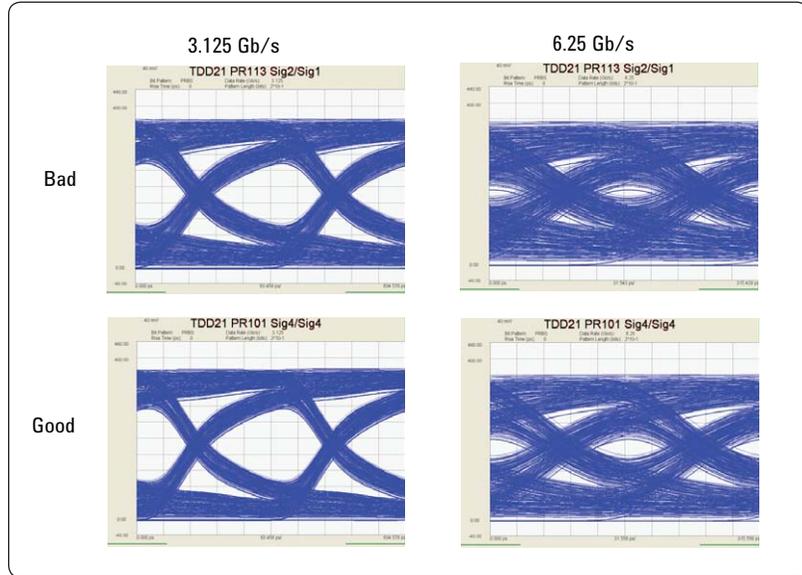


Figure 26. eHSD Eye Diagrams

The best eHSD channel uses N4000-13si with signal layer 4 on the line card and signal layer 4 on the backplane. The worst channel uses daughter card signal layer 2 and backplane signal layer 1. As previously mentioned, signal layer 1 on the backplane has a via stub of over 60 mils. Although the effects of the signal degradation are barely discernable at 3.125 Gb/s, the eye is substantially affected at 6.25 Gb/s.

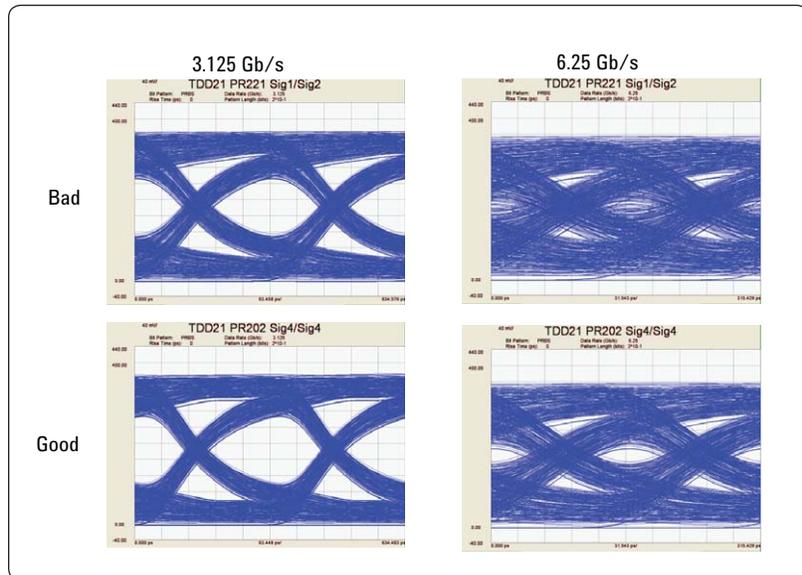


Figure 27. HM-Zd Eye Diagrams

Eye Diagram Analysis (cont'd.)

For the HM-Zd connector channels the best channel uses the bottom layer on the daughter card, and a lower backdrilled layer on the backplane. Given that the backplane layer is N4000-13si, the attenuation due to dielectric material loss is minimized on this channel also. The worst channel uses the top layer on the daughter card, and an upper signal layer on the backplane. This channel uses signal layer 2 on the backplane. This layer is one of the upper layers that is above the region that can be backdrilled. Therefore it has a significant via stub that impacts the overall performance of the channel.

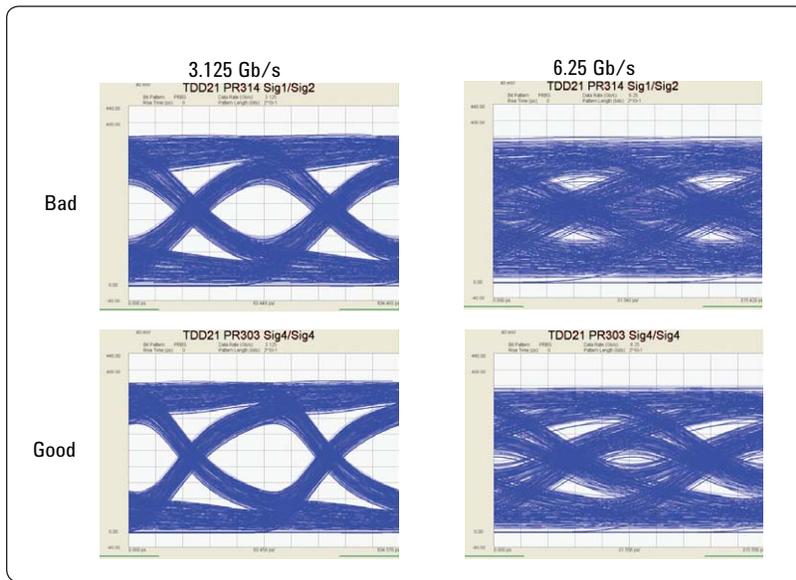


Figure 28. HM-2mm Eye Diagrams

For the HM-2mm connector the best channel is routed on the bottom signal layer on the daughter card, and on the lower Nelco4000-13si layer on the backplane. This backplane layer is backdrilled to a minimal stub length. Even with these advantages, the eye opening of the best channel at 6.25 Gb/s is almost closed. Even with the lack of performance of these channels, at 3.125 Gb/s the channel appears serviceable.

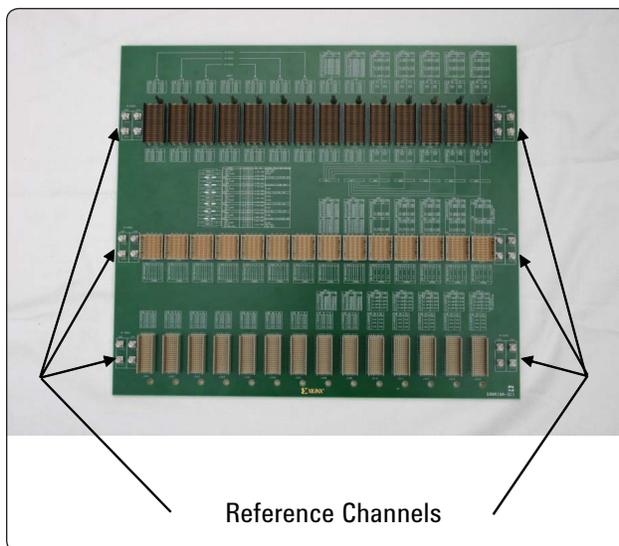


Figure 29. Backplane Reference Channels

Reference Channels

As mentioned previously, there is a reference channel on the backplane for each of the routing layers. These reference channels use an SMA connector for signal launch. Each reference channel is routed as a balanced differential signal pair and uses the same trace geometry as that of the traces on that layer that run between the backplane/daughter card connectors. With the exception that for a short distance the traces are routed from the SMA connectors as single ended traces before they are transitioned to a balanced differentially coupled trace pair. Since there are six signal layers on the backplane, there are six reference channels.

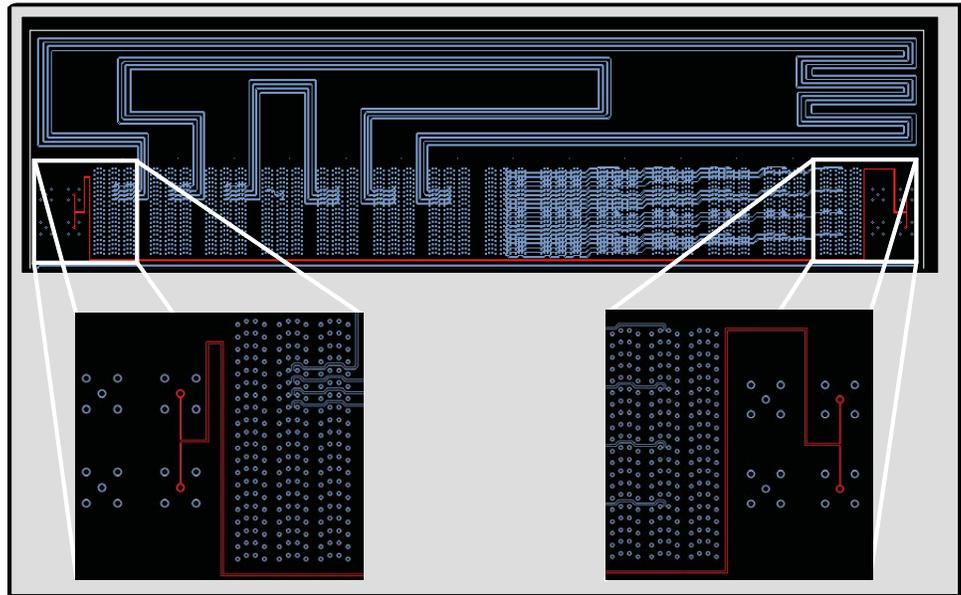


Figure 30. Reference Channel Routing

Figure 30 shows the routing for one of the reference channels. As you can see, there is a short distance where the traces are routed as striplines before they transition to differential striplines. As differential striplines, the reference channels use the same trace geometry, width and separation, as is used for the other traces on that signal layer. The total length of each reference channel trace is 20 inches.



Figure 31. Reference Channel Insertion-Loss

The insertion loss on one of the reference channels is shown in Figure 31. There is a resonance at approximately 9.7 GHz. This resonance does not appear in the other channels routed on this layer. As mentioned previously, the trace geometries for the reference channel are that same as those of the other signals on this layer. Therefore the investigation focused on the SMA connector launch. The via barrel geometry has a different diameter from that of the compliant pin vias for the backplane connectors. More significant is the fact that the pin depth for the SMA connector is much greater than that of the backplane connectors. Whereas, the backplane connector pin depth is on the order of 50 mils, the reference channel SMA pin depth is more than 190 mils. So even though the via barrels for the reference channel SMA connectors were backdrilled to the same depth at each layer as those of the compliant pin backplane connectors, the SMA signal pin was acting as a stub.

Reference Channels (cont'd.)

To address the issue of the SMA compliant pin generating a stub, the center pin on the SMA connector was trimmed to approximately 50 mils. Figure 32 is a photograph of an SMA connector with the center pin trimmed and an SMA connector with the center pin untrimmed. Figure 33 is a diagram of the compliant pin SMA connector mounted in the backplane with a trimmed and untrimmed center pin. The diagram shows that the untrimmed connector extends beyond the backdrilled via barrel while the trimmed connector does not extend beyond the backdrilled via barrel.

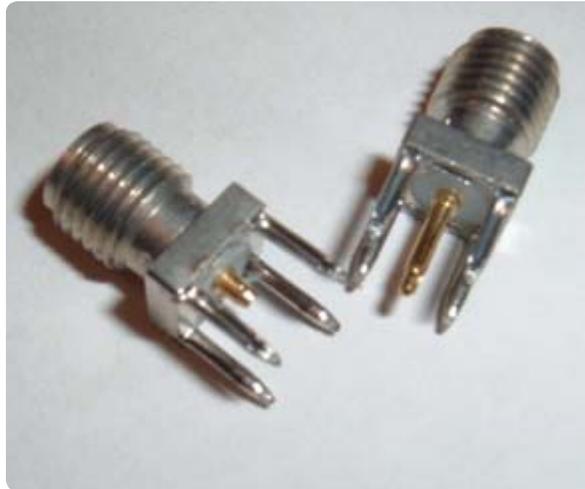


Figure 32. Trimmed and Untrimmed SMA Connectors

With trimmed and untrimmed connectors the insertion loss measurement was repeated. The tests were performed with the reference channel connectors on one side of the reference channel trimmed and with both of the reference channel connectors trimmed. As can be seen in Figure 33, the resonance is eliminated by trimming the center pin of all of the SMA connectors.

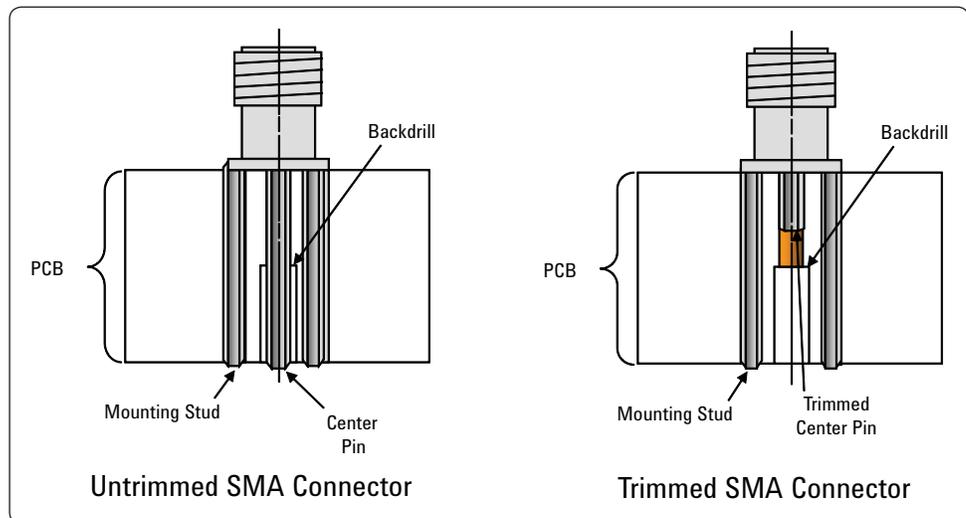


Figure 33. SMA Connector Pin Stub Diagram

Figure 34 shows the effects of the SMA connector pin stub on the eye diagram at 3.125 Gb/s and at 6.25 Gb/s. Although the affect is noticeable at 6.25 Gb/s, the difference in the performance of the channel at 3.125 Gb/s between the trimmed and untrimmed connector pin is barely perceptible.



Figure 34. Reference Channel Insertion Loss with Trimmed SMA

As shown in Figure 35, the eye diagram is barely discernable at 3.125 Gb/s. It is noticeable at 6.25 Gb/s. At 10 Gb/s, it has much more affect. The SMA connector stub caused a resonance at 9.7 GHz. Even at 10 Gb/s, the fundamental bandwidth is only 5 GHz, and because the resonance primarily affected the region around 9 to 11 GHz, the eye for the 10 Gb/s signal still had a healthy fundamental and third harmonic response for passing the data.

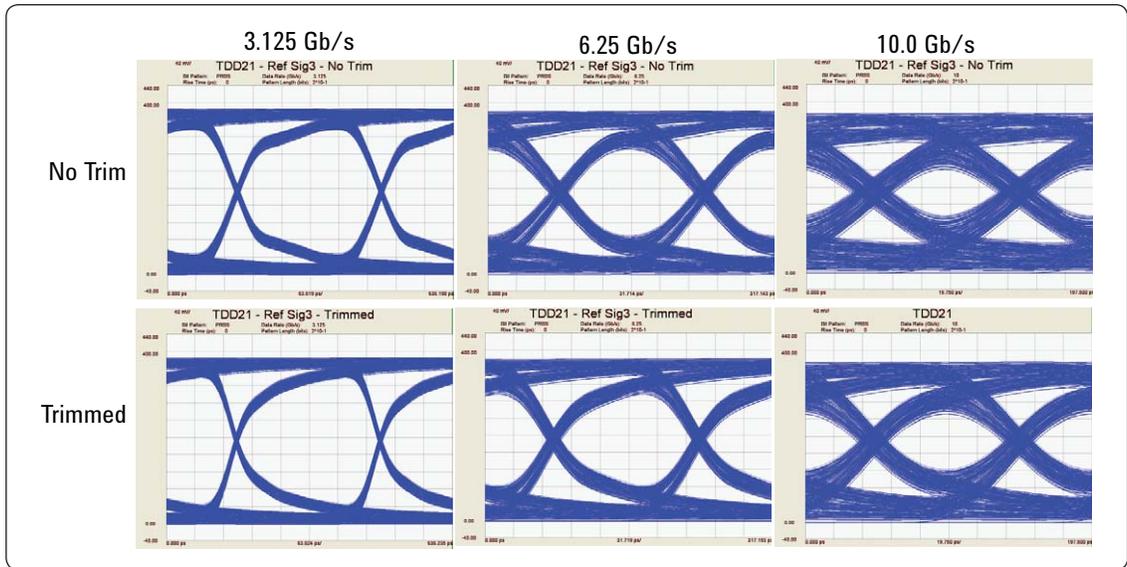


Figure 35. Eye Diagrams for Reference Channel

Summary

The backplane demonstration platform was built to provide a range of channel behaviors. By using a variety of connectors, PCB board materials, PCB routing structures, and routing paths, a range of channel behaviors was achieved. These channel behaviors were characterized and analyzed using a 12-port VNA. The stub length on the connector vias had a significant affect on channel behavior. The crosstalk test and analysis showed that most of the crosstalk appeared in the backplane connector via field. Although some of the channel responses appeared to be suspect, the eye diagram analysis showed that a serviceable eye opening can be achieved with over 36 inches of daughter card and backplane trace length for most of the channels at bit rates up to 6.25 Gb/s.

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