Agilent *Medalist* i3070 Test Throughput Optimization

Application Note

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This application note explores some factors which cause test time to increase on the *Medalist* i3070 In-Circuit Test system, and methods which users can employ to reduce the test time and increase throughput on the *Medalist* i3070 ICT system.

Why does test time increase?

Longer test times can arise from a variety of issues:

1. The test generated from the Interactive Program Generator (IPG) may not be optimized for the specific production board revision.
2. Addition of test options when debugging the tests the first time.
3. Addition of test options during production testing.
4. Incorrect interrupt analog test.
5. Incorrect power up.
6. Using default vector cycle to test digital devices.
7. Overly long wait during powered test.
8. Using “safeguard cool” command arbitrarily.
9. Overly complex test.
10. Immoderate wait in “testplan” file.
11. Incorrect GP-Relay usage.
12. Poorly maintained i3070 system hardware.

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Optimizing test programs for the i3070 ICT system.

The i3070 ICT software offers various tools to help test engineers optimize their programs step-by-step.

1. Pins Test

The Pins Test verifies if there is good contact between the fixture and the printed circuit board currently being tested. Here is the syntax in the "testplan":

1) The Pins Test is controlled by setting a flag in the "Set_ Custom_Options" subroutine.
2) Find the Chek_Point_Mode flag in Set_Custom_Options routine. It can be set to OFF, PRETEST or FAILURES. (e.g.: Chek_ Point_Mode = Failures)
   - OFF - Do not use Pins Test at all.
   - PRETEST - Run the Pins Test on every board, as the first test.
   - FAILURES - Run the Pins Test only after a failure has been detected.

Ideal setting for Pins Test usage:
Only run Pins Test when a failure has been detected (Chek_Point_ Mode = Failures). This is the default mode.

2. Shorts Test

A very important setting to take note of in the Shorts Test is settling delay time. The default setting for settling delay is 50.00u. This means there will be a 50 microsecond delay in between every node.

Ideal setting for Shorts Test:
Try to set settling delay at 0 first, or comment all settling delay sentences in debugging. Depending on actual conditions, et enough settling delay time.

Real-time example:
Using default settling delay, shorts test time was 5.563 seconds. After optimizing settling delay, shorts test time was reduced to 2.094 seconds.

For example:

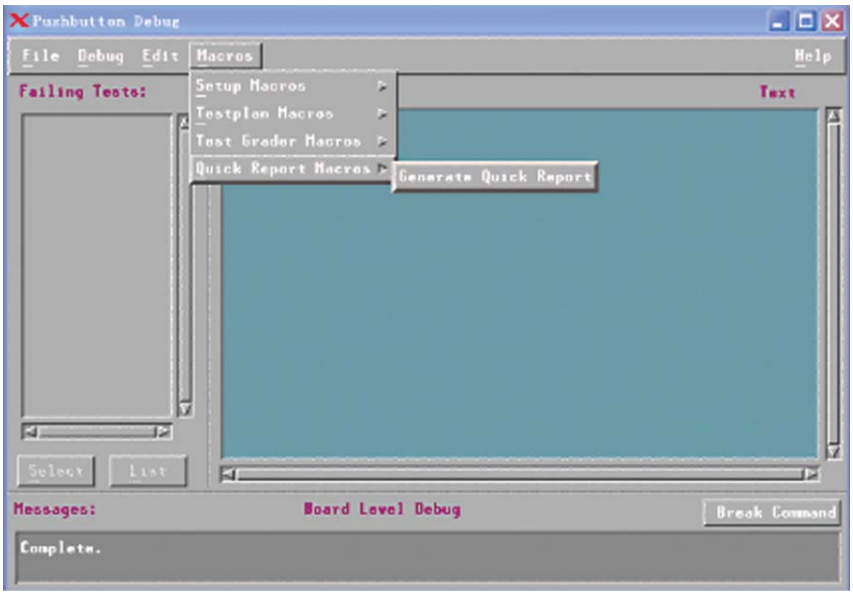
```
report netlist, common devices
!!************************************************
threshold      15
!settling delay 50.00u
short "SMVREFCAP" to "SMVREFSOURCE"
short "UNNAMED_44_CAP_I136_A" to "FE0_RX-"          !J4
short "UNNAMED_44_CAP_I136_A" to "FE0_RX+"          !J4
short "UNNAMED_44_CAP_I135_A" to "FE0_TX-"          !J4
short "UNNAMED_44_CAP_I135_A" to "FE0_TX+"          !J4
short "V2P5_DCAP4" to "V_2P5"
    !u27
short "H_GTLREF_MCH" to "H_GTLREF_MCH_A7"           !u13
... ...
report phantoms
threshold      1000
!settling delay 6.165m
nodes "FAN_FB1"
!settling delay 55.00u
nodes "UNNAMED_56_CAP_I163_B"
nodes "PSU_TEMP"
... ...
settling delay 1m
nodes "UNNAMED_46_LTC4210_I46_SENSE"
nodes "UNNAMED_41_CAP_I65_B"
nodes "UNNAMED_39_CAP_I155_B"
nodes "UNNAMED_16_ICS952601_I182_P33V"
nodes "UNNAMED_16_CAP_I161_A"
nodes "VCC3.3_CLK"
nodes "P3_3V"
nodes "V_1P25MEMVTT_B"
        ... ...
```

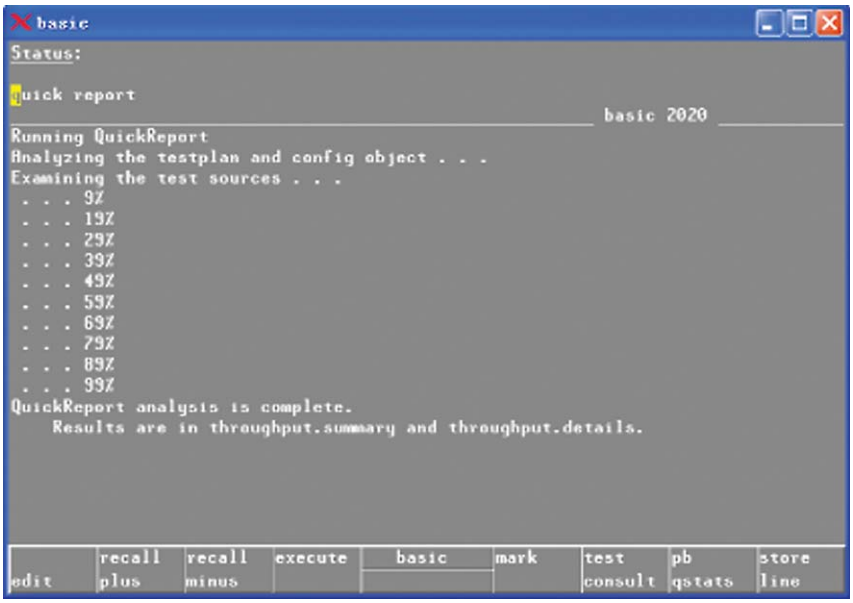
3. Quick Report

The Quick Report evaluates a board directory, identifies areas where changes could be made to reduce test time, and suggests strategies to maximize throughput. You can use the information to determine how to adjust your tests, testplan, and system resources to reduce test times and increase throughput.

Quick Report can be generated by PushButton Debug Macros or in BT-Basic window.

Quick report will generate two files, “throughput.summary” and “throughput.details”, under the board directory.





4. Analog Options

Some analog test options can increase test stability; however, they can also increase the test time. Examples of such analog test options are:

1) Wait options – wa, dwa
2) 6-wires test – sa, sb, sl, en
3) Line noise rejection – ed

The following analog test options will not incur time penalty: am, ar, fr, of, ico, op, pf, pm, re, sm, wb

Wait Options

wa: Wait option delays the test for the specified time (X seconds) to allow reactive components to stabilize. Do note that the “wa” option is a source wait!

- This wait is executed each time the voltage source is changed. After the signal is applied, a wait is enforced.
- A second wait is encountered when the voltage source is turned off. This allows reactive devices in the test circuit to discharge any power that might have been accumulated during the test.

The total time added to the test is twice the time specified for “wa”.
dwa: Wait option delays the test for the specified time (X seconds) while the device stabilizes. It differs from the wait statement in that the delay is only applied before testing. Do note that the “dwa” option is a detector wait!

6-Wires Test
Here is an overview of the 6-wire tests:

sa: Senses the source voltage being applied to the component under test.

sb: Senses the detector voltage.

sl: Senses the guard point.

en: This enhancement option obtains multiple measures of the device and the measurement circuit in the following manner:

- The actual voltage output of the voltage source (V_S) is measured.
- The voltage at the input of the Measuring Operational Amplifier (MOA VI) is measured.
- The voltage drop across the Reference Element is measured.
- Finally, V_{MOA} is measured.

It can be seen that a component test using the "en" option is going to take much longer than the same test that does not use "en".

Line noise rejection:
ed: Line Noise Rejection is used to integrate the measurement over a line cycle. This results in a more stable measurement if the cause of instability is due to line noise.

The default measurement integration time is 500us. If "ed" is used, the integration time is increased to 20ms for50Hz systems, and 17.5ms for 60Hz systems.

Reducing redundant test options to save test time
The best method is to remove extra test options, and use more guarding to ensure stability during analog test. For example:

If other remote sensing or scanner sensing is present, you can turn them off.

If the"fr128" option has been set, change it to "fr1024", and remove the "ed" option.

If the "en" option has been set, remove it.

If the "wa" or "dwa" option has been set, reduce the wait time, or remove it.

AutoOptimizer – New feature available with i3070 software revision 07.00 and above
The i3070 software revision 07.00 and above comes with AutoOptimizer - a new tool for analog test optimization. Do note, however, that AutoOptimizer usage can only be enabled with a Control XTP card.

DC Source Voltage	Total Test Time	AC Source Voltage	Total Test Time
1 test @ 500us/test	500µs	2 tests @ 500us/test	1.0ms
8 tests @ 500us/test = 4ms Adding only "en", and no other options. Measuring VS, VI, VRE and VMOA with specified source applied and with source set at 0 volts.	4ms	12 tests @ 500us/test = 6ms Measuring VS, VI, VRE and VMOA for the Imaginary signals (+90 and -90) and for the Real signal.)	6ms
Integration time for adding "ed" (with no other options	20ms	Integration time for adding "ed" (with no other options).	20ms
Adding en test: 8 en tests @20ms	160ms	Adding en test: 12 en tests @20ms	240ms
Adding ed, en: Waiting time to apply signal = 10ms 8 en tests @20ms each = 160ms Waiting time for signal removal = 10ms	180ms	Adding ed, en: Waiting time to apply signal = 10ms 12 en tests @20ms each = 240ms Waiting time for signal removal = 10ms	260ms

Table 1: Illustration of how extra test options result in significant increase in test times.

5. Power Up Sequence

1) Use the "optimize" option for parallel power up, if DUT board is independent of power sequence. This is the default setting for IPG generate testplan.
2) Avoid "wait" option or reduce "wait" time.

6. Digital Test Optimization

Optimizing the vector cycle Digital test is based on vector time, hence any reduction of the "vector cycle" can save digital test time.

Occasionally, the "vector cycle" and "receive delay" times are not defined in the digital test. In such cases, the i3070 system will use the default vector time – 500ns.

The i3070 has three testhead options:

i3070 Testhead Options	Testhead Speed	Range
Standard system	6MHz	160 nanoseconds to 1.59 ms
Advanced system	12MHz	80 nanoseconds to 1.59 ms
High accuracy system	20MHz	50 nanoseconds to 1.59 ms

Boundary scan and Silicon Nails test will spend many test time.

As an example, on a 6MHz i3070 system running a one boundary scan test with 80,000 vectors using the default vector cycle setting, the test time is 40.0 milliseconds. By reducing the "vector cycle" to 160ns on a 6MHz i3070 system, the test time is slashed to 12.8 milliseconds.

Using "Safeguard Cool"

What is "Safeguard Cool"?
The Safeguard Cool" feature applies a cool down delay between tests. Digital tests are inhibited during this period for safety reasons, but the cool-down delays are enforced. Essentially, any Safeguard Inhibits command is ignored.

DO NOT use "safeguard cool" for every digital test!

The "compile "digital/IC_Name"; list" is good tool to check which digital IC requires "safeguard cool".

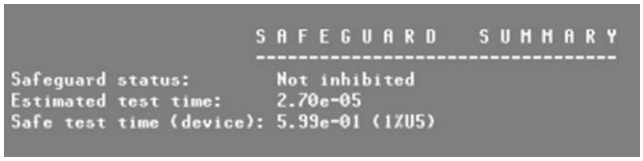


Figure 1: This screenshot shows an example of a digital IC that does not require "Safeguard Cool"

Figure 2: This screenshot shows an example of a digital IC test that has been inhibited by Safeguard, because the test time is too long. In such a case, "Safeguard Cool" can be used to proceed with the test.

Figure 3: This screenshot shows an example of a digital IC test inhibited by Safeguard, because the upstream device is not a digital device. If the analog device is ignored, the "Safeguard Digital" test option can be used.

Note: Be careful if a transistor is driving a digital input and the safeguard level has been set to digital. Will the digital driver damage the transistor? Probably not, but you may want to adjust your driver levels to limit the amount of current the transistor has to source or sink.

Reducing extra Wait Time
Do not add superfluous "wait" in digital test. Check all the "wait" options in every digital test and either reduce or delete it accordingly.

Overly Complex Libraries
Sometimes, digital libraries can become too complex. The test engineer can reduce some unused tests or re-generate a new library during debug.

Faster On-Board Programming
For existing test programs, use "flash isp" for faster test compared with "flash", or use "flash" instead of "sequential to speed up the test. In addition, enabling "flash 70" and "FF stripping" can accelerate the test.

Mixed Test
Reduce the number of "continue analog" and "continue digital" statements.

7. Testplan optimization

1) Do not interrupt analog tests. The test controller will download all objective files into the RAM. If the test is interrupted, the test controller will re-download the objective files from the point of interruption. Instructions such as "unpowered", "powered" and "if...then..." can interrupt the analog test.
2) Reduce or delete "wait" time in the testplan.
3) Reduce "GP-Relay" usage. 4) Do not use same "GP-Relay" repeatedly!
4) Do not add "Safeguard Cool" at the beginning of the subroutine. The i3070 system default setting is "Safeguard All" for every subroutine. So, realign the digital test sequence for the safeguard settings. For example:

```
sub Digital_Tests (Status_
Code, Message$)
global Status
    if Message$ <> "" then
    print tab(5);Message$
    Status = Status_Code
    test "digital/u14"
    test "digital/u46"
    test "digital/u47"
    ... ...
    safeguard digital
    test "digital/u101"
    test "digital/u110"
    ... ...
    safeguard cool
    test "digital/u53"
subend
```

5) Use the simplest testplan for your test, and remove or comment out the unnecessary sentences in your testplan.

8. Upgrade your legacy 3070 hardware and purchase a license for the latest software with the fastest speeds.

Your legacy 3070 system hardware can lead to a significant increase in your test time due to the more complex boards it has to test today!

Agilent's latest PC controller provides more stable and faster running time. Here are some highlights of what the latest Agilent *Medalist* i3070 suite can offer you:

- ASRU C Revision and Control XTP provide one of the fastest tests in the industry.
- 12 MHz or 20 MHz Hybrid Double Density Cards provide unparalleled speed and coverage
- Additional features available with latest i3070 software revisions 07.1 and above.
- Panel test license.
- Throughput Multiplier license.
- Flash 70 license.
- Flash ISP license.

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