Two-Stage 800 – 1000 MHz Amplifier Using the AT-41511 Silicon Bipolar Transistor

Application Note 1084

Introduction

Commercial markets in the VHF through L band frequency range require low cost, high performance components. In many applications, such as cellular and pager, a bipolar transistor must provide low noise pre-amplification at very low current consumption since battery power is at a premium.

This Application Note describes the performance of the Hewlett-Packard AT-41511 low cost low noise bipolar transistor. The AT-41511 is used in a two stage low noise amplifier in the 800 to 1000 MHz frequency range. The amplifier is designed around the catalog S Parameters at a V_{CE} of 8 volts and a collector current, I_C, of 10 mA. Although designed for operation at a V_{CE} of 8 volts, the amplifier has very good performance as a low noise amplifier at collector voltages as low as 3 volts. The amplifier also provides a means of generating moderate power at a V_{CE} of 5.5 volts.

Circuit Design

Using Touchstone™, a two-stage amplifier was designed to provide a nominal 2 dB noise figure and 30 dB of stable gain. A completed amplifier showing component placement is shown in Figure 1.

Active biasing is used to set the quiescent bias point of each stage, although typical four resistor biasing could be used with reduced performance over temperature. The active bias assures that the bias point will remain relatively constant regardless of changes in dc parameters from device to device.

The artwork including placement of the plated through holes is shown in Figure 2. The artwork measures 2.05 inches by 1.5 inches. A schematic diagram is shown in Figure 3.

The amplifier is designed for use with inexpensive 0.062 inch thickness FR-4/G-10 epoxy glass dielectric material.

The schematic diagram in Figure 4 shows the bias components that would be used if resistor biasing is used. The values shown in the schematic are typical for a 3 volt power supply voltage and each device set at a V_{CE} of 2.7 volts and I_C of

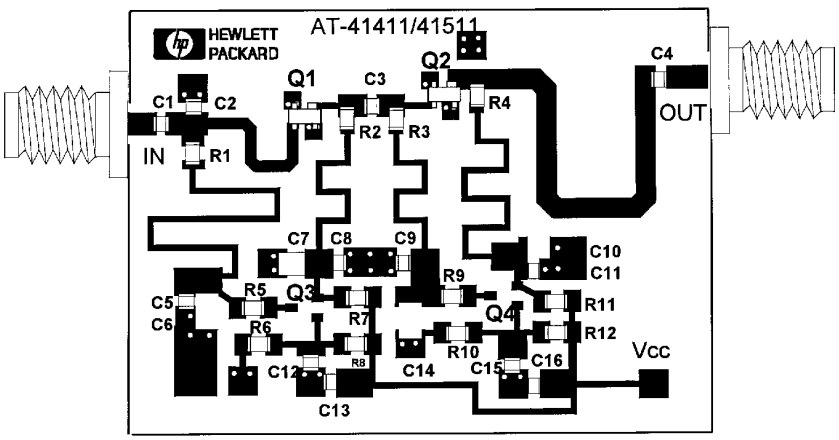
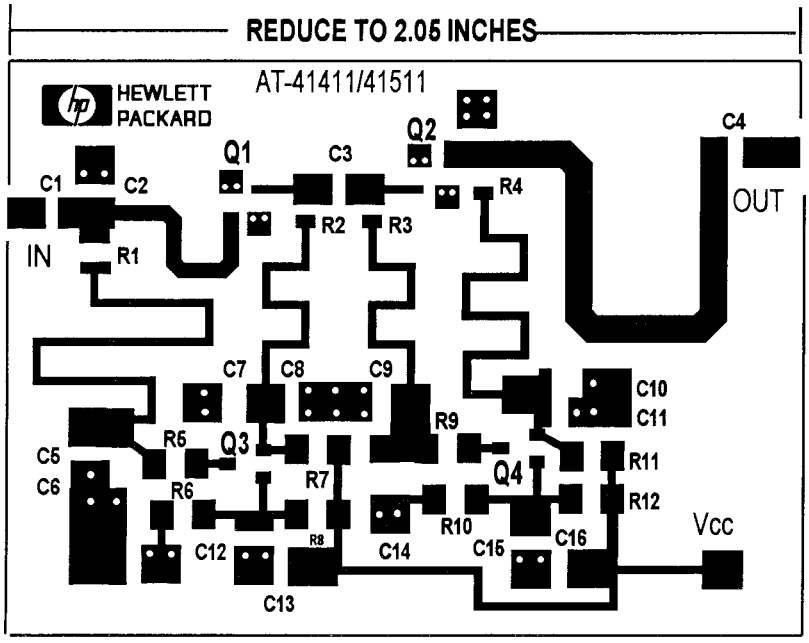
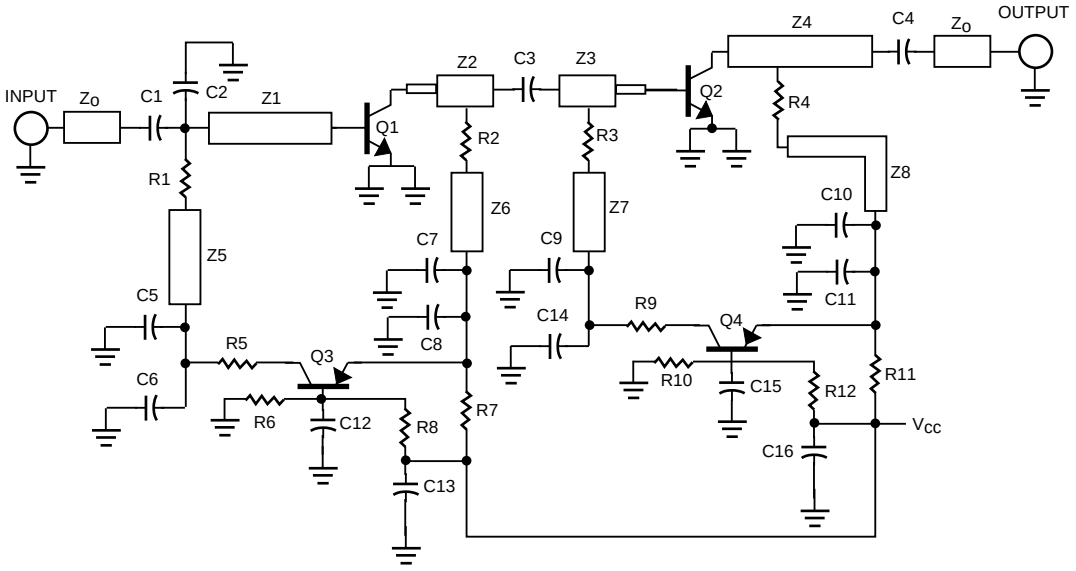


Figure 1. Complete 900 MHz Two-Stage AT-41511 Amplifier showing component placement. (Enlarged for clarification. Actual size: 2.05 inches by 1.5 inches.)



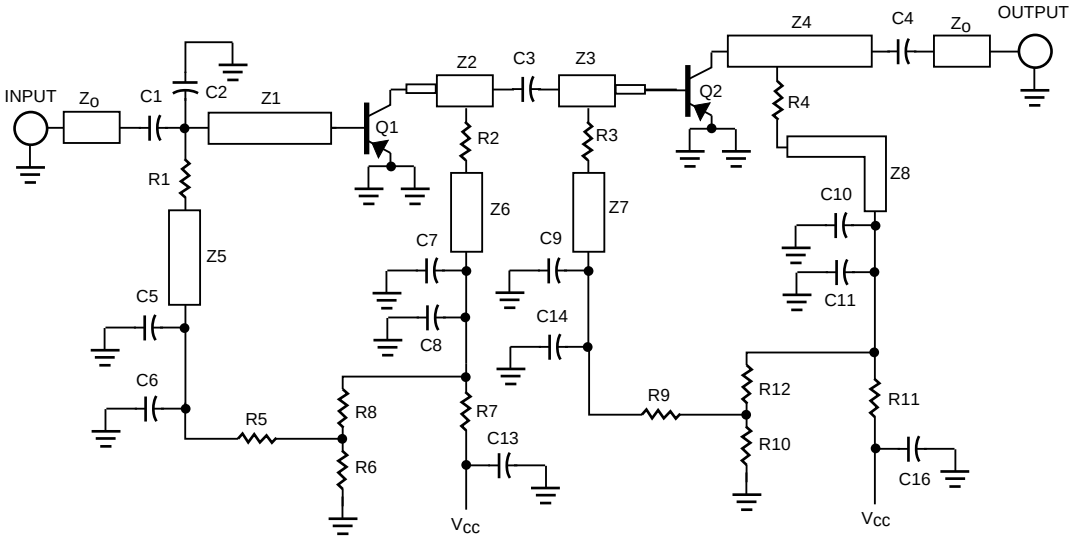
WARNING; DO NOT USE PHOTO-COPIES OR FAX COPIES OF THIS ARTWORK TO FABRICATE PRINTED CIRCUITS.

Figure 2. Artwork for 900 MHz AT-41511 amplifier showing placement of plated through holes. (Shown 2x size)



C1–27 pF CHIP CAPACITOR
C2, C3 – 4 pF CHIP CAPACITOR
C4–5.6 pF CHIP CAPACITOR
C5, C8, C9, C11, C12, C13, C15, C16–1000 pF CHIP CAPACITOR
C6, C7, C14, C10–0.1 μF CHIP CAPACITOR
Q1, Q2 – HEWLETT-PACKARD AT-41511/41411 SILICON BIPOLAR TRANSISTOR
Q3, Q4, – SIEMENS SMBT 2907A PNP TRANSISTOR
R1, R2, R3, R4 – 50 OHM CHIP RESISTOR
R5, R6, R9 – 1.5 K OHM CHIP RESISTOR
R7 – 150 OHM CHIP RESISTOR
R8, R10 – 750 OHM CHIP RESISTOR
R11 – 110 OHM CHIP RESISTOR
R12 – 360 OHM CHIP RESISTOR
Z_O – 50 OHM MICROSTRIPLINE
Z1–Z4 – ETCHED MICROSTRIPLINE CIRCIITRY
Z5–Z8 – MICROSTRIPLINE BIAS DECOUPLING LINES

Figure 3. Schematic of AT-41511 amplifier using active bias for both stages.



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Q1, Q2 – HEWLETT-PACKARD AT-41511/41411 SILICON BIPOLAR TRANSISTOR
R1, R2, R3, R4 – 50 OHM CHIP RESISTOR
R5, R9 – 32 K OHM CHIP RESISTOR
R6, R8, R10, R12 – 2.7 K OHM CHIP RESISTOR
R7, R11 – 86 OHM CHIP RESISTOR
Z_O – 50 OHM MICROSTRIPLINE
Z1–Z4 – ETCHED MICROSTRIPLINE CIRCUITRY
Z5–Z8 – MICROSTRIPLINE BIAS DECOUPLING LINES

V_{CC} = 3 VOLTS

Figure 4. Schematic of AT-41511 amplifier using typical 4 resistor passive biasing for both stages. Each stage is biased at approximately 2.7 volts V_{CE} and I_C of 3 mA with a supply voltage of 3 volts.

3 mA. Some jumpering of etch and slight movement of bias resistors on the original board is necessary in order to connect R8 to the junction of C8 and R7 and to connect R12 to the junction of C11 and R11. Resistors R7 and R11 help set the collector voltage while resistors R5 and R9 set the base current required to support the desired collector current based on nominal h_{FE}.

Test Results

The AT-41511 amplifier circuit was biased up at several power supply voltages in order to analyze the basic circuit at various device V_{CE} and I_C. In the following examples, only the dc parameters were changed. The original RF impedance matching network remained the same throughout all tests.

At a power supply voltage of 3 volts, the V_{CE} of both devices is 2.5 volts. The first stage is biased at an I_C of 2.8 mA while the second stage is biased at an I_C of 3.6 mA. Measured P_{1dB} at 900 MHz is -3 dBm referenced to the output port. The corresponding gain and noise figure as measured between 800 MHz and 1000 MHz is as shown in Figure 5.

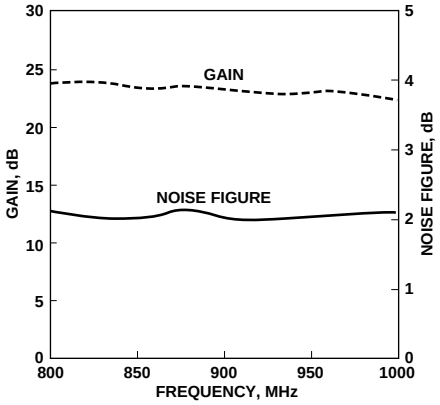

Figure 5. Gain and Noise Figure vs. Frequency at V_{CC} = 3 volts

Increasing the power supply voltage to 6 volts forces V_{CE} of both stages to be approximately 4.1 volts. First stage collector current is 9 mA while the second stage collector current is 12 mA. Measured P_{1dB} at 900 MHz is now +8 dBm referenced to the output port. Figure 6 shows gain and noise figure versus frequency.

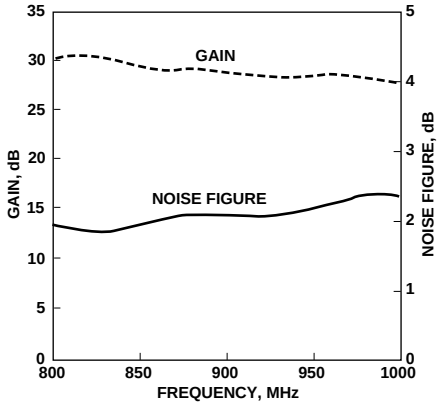

Figure 6. Gain and Noise Figure vs. Frequency at V_{CC} = 6 volts

A comparison between power output vs. quiescent bias point is shown in Table I. The efficiency of the second stage, Q2, is also listed for comparison. The data indicates that the conjugate match provided for Q2 is probably more optimum at the lower collector voltage. Further bench tuning should improve efficiency at the higher collector voltages. It is also important to note that increased efficiency can be had by not using active biasing. Active biasing is excellent for low noise amplifiers but can limit power output by attempting to hold the collector current constant with drive. Increased efficiency can be obtained by allowing the device to transfer into class AB operation instead of class A.

Circuit Variations

The original circuit board was designed for the AT-41411 and AT-41486 devices and will work quite well with these devices also. It may be possible to shorten the output series microstripline to save space and still achieve rated performance with minor tuning.

The ideal bias decoupling line would be a quarter wavelength of high impedance microstrip with a low impedance capacitor placed at the power supply end of the line. This will force a high impedance at the RF circuit side of the line. At lower frequencies the length of line will sometimes become excessive due to layout constraints. One option is to meander the lines as is shown in Figure 1 and 2. Another option is to replace the high impedance line with a high value resistor if the current drawn at this device terminal is not high. This may be possible at the base of the second stage transistor and the collector of the first stage. High values of resistance in the bias lines are not always the best choice, however. Using the quarterwave lines with a series 50 ohm resistor does load the device in 50 ohms at very low frequencies which will improve stability. Using a quarterwave bias line at the input to the first stage is the best solution if lowest noise performance is desired. As always, tradeoffs between simplicity and circuit performance must be considered if success is to be obtained.

The 0.1 µF capacitors in parallel with the 0.001 µF capacitors in the bias circuit may not be required in all locations. They are used to minimize noise generation in the PNP transistors used in the active bias scheme.

Table I. Power output vs. bias point for 2-Stage AT-41511 Amplifier.

Device	V_{CE} (volts)	I_C (mA)	P_{1dB} (dBm)	P_{1dB} (mW)	Q2 Efficiency
Q1	2.5	2.8	---	---	
Q2	2.5	3.6	-3	0.5	5.5%
Q1	4.1	9	---	---	
Q2	4.1	12	+8	6	12.2%
Q1	3.7	19	---	---	
Q2	3.4	25	+13	20	23.5%
Q1	4.4	18	---	---	
Q2	4.3	24	+14	25	24.3%
Q1	5.1	24	---	---	
Q2	5.0	33	+15	32	19.4%
Q1	5.6	27	---	---	
Q2	5.5	38	+16.5	45	21.5%

Conclusion

This application note has described a two-stage silicon bipolar amplifier for the 800 to 1000 MHz frequency range that provides a means of providing low noise preamplification with low current consumption. The same amplifier also provides a means of generating moderate power at increased power consumption.

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