Low Noise Amplifiers for 320 MHz and 850 MHz Using the AT-32063 Dual Transistor

Application Note 1131

Introduction

This application note discusses the Hewlett-Packard AT-32063 dual low noise silicon bipolar transistor. The AT-32063 consists of two AT-320XX transistors mounted in a single package with all terminals brought out separately. This concept allows the designer flexibility with circuit design. The AT-32063 is packaged in a low cost SOT-363 (SC-70) plastic surface mount package and is available in Tape-and-Reel for high volume applications.

The device is analyzed in several low noise amplifier applications in the 300 to 900 MHz frequency range. With the low current consumption of the AT-32063, the device makes an ideal low noise front-end for pager and cellular applications.

Circuit Topologies

The AT-32063 dual transistor can be used in a variety of applications. The most common application would be use as an amplifier. Several circuit topologies exist. These include a common emitter stage driving a second common emitter stage, the Darlington configuration where both collectors are connected together, and the cascode arrangement. The cascode configuration will be the subject of this application note. The cascode consists of 2 transistors. One transistor is operating in a common emitter configuration followed by a second transistor operating in the common base configuration. When properly designed this configuration has the advantages of good stability and a very high output impedance which can be set by the output load impedance.

850 MHz Circuit Design

The 850 MHz amplifier is designed for operation from a 2.7 V power supply with a total collector current of either 1 or 2 mA. The amplifier schematic diagram is shown in Figure 1. The first transistor connected as a common emitter has its emitter hard grounded for both good RF performance and a dc ground.

The input matching network is designed for low noise. The collector of the first stage is dc connected to the emitter of the common base stage such that current can be shared. Biasing both devices in series requires that the base of the second stage be dc floating but RF bypassed. When a transistor is operated in a common base configuration, the inductance associated with the base bond wire is often long enough to place the transistor in a negative resistance region somewhere in the 2 to 4 GHz frequency region. This effect can be negated by the addition of a series resistor between the base lead and the RF bypass capacitor.

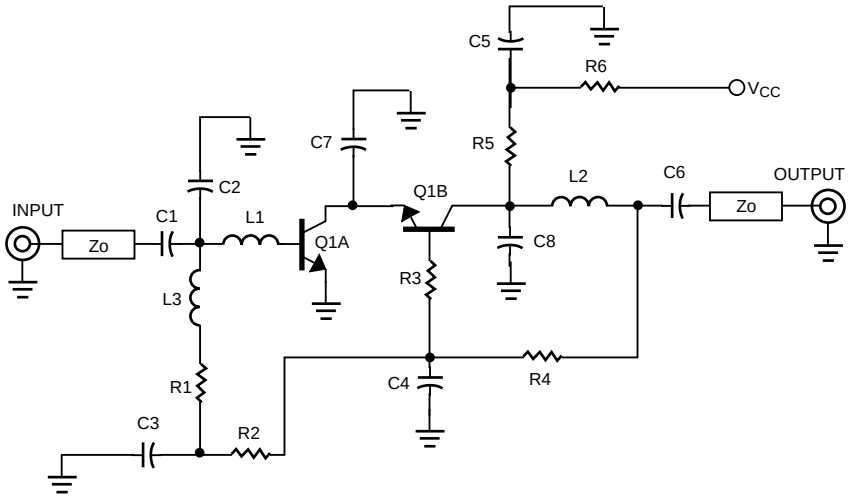
Adding resistance in the base lead of Q1B does have the adverse effect of decreasing the power output capability of the amplifier. A resistor in the range between 22 Ω and 50 Ω is a good starting value. It was found empirically that decreasing the value of R3 to 15 Ω increased the output IP3 by 1 dB. The actual value will be a tradeoff between desired gain, stability both in-band and out-of-band and power output.

With the high output impedance of the common base stage, a shunt resistor is used to control the gain and ultimately the stability. In the 850 MHz amplifier, a 360 Ω resistor bypassed to ground provides a constant impedance to the second stage.

An impedance matching network consisting primarily of a shunt capacitor (C8) and a series inductor (L2) provides an imped-

ance match to 50 Ω. Depending on the selection of a power supply voltage, an additional resistor at R6 may be required. Typically, the voltage required on the power supply end of the 360 Ω resistor, R5, is in the 2.7 to 3.2 volt range depending on current consumption. A higher voltage power supply will necessitate the use of R6 to drop the voltage to the nominal 3 volts.

A Touchstone simulation and performance printout are shown in Appendix A.



C1 = 12 pF CHIP CAPACITOR
C2 = 0-2 pF CHIP CAPACITOR (ADJ FOR NF/VSWR), C2 = 0 DEMO PCB
C3, C5 = 1000 pF CHIP CAPACITOR
C4 = 100 pF CHIP CAPACITOR
C6 = 22 pF CHIP CAPACITOR
C7 = MAY BE USED TO TUNE POWER OUTPUT
C8 = USED TO TUNE OUTPUT VSWR - NOT USED ON DEMO
L1 = 12 nH CHIP INDUCTOR (COILCRAFT 1008CS-120)
L2 = 22 nH CHIP INDUCTOR (COILCRAFT 1008CS-220)
L3 = 180 nH CHIP INDUCTOR (COILCRAFT 1008CS-181)
Q1 = HEWLETT-PACKARD AT-32063 DUAL SILICON BIPOLAR TRANSISTOR
R1 = 50 OHM CHIP RESISTOR
R2 = 150 - 330K OHM CHIP RESISTOR (ADJUST FOR RATED I_C)
R3 = 15 - 50 OHM CHIP RESISTOR (50 OHM ON DEMO BD.)
R4 = 22 K - 47 K OHM CHIP RESISTOR (SETS V_{CE1} AND V_{CE2})
R5 = 360 OHM CHIP RESISTOR (INCREASE FOR HIGHER IP3, SEE TEXT)
R6 = OPTIONAL RESISTOR DEPENDING ON SUPPLY VOLTAGE (SEE TEXT)
Zo = 50 OHM MICROSTRIPLINE

Figure 1. Schematic Diagram and Parts List for AT-32063 850 MHz Amplifier.

Table 1. AT-32063 Amplifier Performance
V_{ce1} = 0.8 V, V_{ce2} = 1.2 V, I_c = 2 mA

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
500	16.9	1.36
520	16.2	1.46
540	16.1	1.56
560	17.1	1.32
580	17.9	1.28
600	16.3	1.27
620	16.9	1.25
640	18.2	1.25
660	17.8	1.22
680	17.7	1.21
700	18.3	1.32
720	17.6	1.21
740	18.0	1.21
760	18.6	1.22
780	18.1	1.31
800	18.1	1.28
820	18.2	1.25
840	18.3	1.25
860	18.1	1.35
880	17.8	1.54
900	17.6	1.43
920	17.3	1.39
940	16.8	1.45
960	16.7	1.53
980	16.0	1.57
1000	15.6	1.63

Test Results

The performance of the prototype amplifier board, as measured on an HP 8970 Noise Figure Meter, is shown in Tables 1 and 2. Two different bias conditions are shown.

The first bias condition is set up for operation from a nominal 2.7 volt power supply. Nominal bias current is 2 mA which is shared by both Q1A and Q1B. The voltage division between Q1A and Q1B is governed by R4 and R2. Since R2 also controls the base current through Q1A, there is interaction between trying to set the device voltage and current. At the expense of increased current consumption, a resistor added in parallel with C4 will act as a voltage divider off the power supply which can be used to force the collector voltage of Q1A to be 1 volt.

The second set of Gain and Noise Figure data is taken at a bias point of 1 mA and $V_{ce1} = V_{ce2} = 1$ volt. See Table 2.

The graphs shown in Figures 2 and 3 show the swept input and output return loss as measured on an HP 8757 Scalar Network Analyzer. The two bias points are shown for comparison.

Table 2. AT-32063 Amplifier Performance
$V_{ce1} = V_{ce2} = 1$ V and $I_c = 1$ mA

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
600	11.8	1.72
640	14.0	1.70
680	13.5	1.59
720	13.7	1.75
740	14.4	1.75
760	14.9	1.53
780	14.5	1.61
800	14.5	1.66
820	14.6	1.56
840	14.8	1.55
860	14.6	1.62
880	14.4	1.70
900	14.2	1.77
920	14.0	1.69
940	13.5	1.75

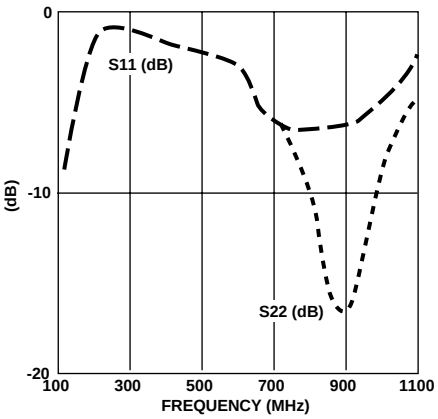


Figure 2. Swept Response at $I_c = 2$ mA

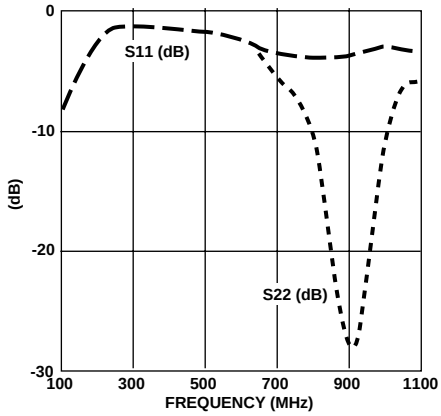


Figure 3. Swept Response at $I_c = 1$ mA

The amplifier provides a nominal gain of 18 dB at an I_c of 2 mA and a nominal 14.5 dB at $I_c = 1$ mA. The input return loss is somewhat better at the higher current. The output return loss is relatively independent of bias current because of the high output impedance of Q1B. The several thousand ohm output impedance is swamped out by the 360 Ω resistor R5. Inductor L2 and a slight amount of capacitance at C8 provide the impedance transformation to 50 Ω. Without any capacitance at C8, the output return loss of the demo amplifier measured between 17 and 28 dB at 900 MHz depending on bias current. The output return loss at 850 MHz is 10 dB and can be improved by adding 0.5 pF at C8. The output match can be easily tuned for any frequency in the 100 MHz through 1 GHz range by merely scaling L2 and C8.

The amplifier intercept point was measured at two frequencies, one at 805 MHz where the output return loss is 10 dB and at 900 MHz where the output return loss measured 28 dB. Bias current is 2 mA. Output IP3 measured +5.5 dBm at 805 MHz and +6 dBm at 900 MHz. The frequency at which best IP3 was observed occurred at the same frequency of best output return loss. This is probably due to the heavy resistive loading used at R5. Output P1dB was also measured to be -11 dBm at 900 MHz. This suggests a difference between IP3 and P1dB of 17 dB.

When the bias is reduced to 1 mA, the output IP3 at 900 MHz was measured at +2 dBm with a corresponding 1 dB gain compression point of -16 dBm. Greater power output should be possible by increasing the value of R5 and shunting an RF choke across R5 to minimize the dc voltage drop. L2 will most likely need to be increased in value in order to match the resultant higher output impedance.

300 MHz Amplifier No. 1 Circuit Design

The 300 MHz amplifier is designed for operation from a 2.7 V power supply with a total collector current of only 600 μA. The existing S and Noise Parameters for 1 V and 1 mA current were used for the initial design. Measuring noise parameters at lower VHF frequencies becomes increasingly more difficult because the device impedances become very large. The large impedances introduce additional error and uncertainty in the measurements. An alternative to time consuming measurements is to use existing data and extrapolate new data for the lower frequencies. Although approximate, the new noise parameter data gave an excellent first approximation to

Table 3. Noise Parameters at $V_{ce} = 1$V and $I_c = 1$ mA

Frequency (MHz)	Fmin(dB)	Γo (mag)	Γo (ang)	Rn/50
250	0.5	0.90	12	0.65
500	0.5	0.80	25	0.55

the noise match required at 300 MHz. Noise Parameters at 250 MHz and 500 MHz were inserted into the existing S and Noise Parameter data for the AT-32063. The new parameters at V_{ce} = 1 V and I_c = 1 mA are shown in Table 3.

The schematic diagram and parts list of the 300 MHz amplifier are shown in Figure 4.

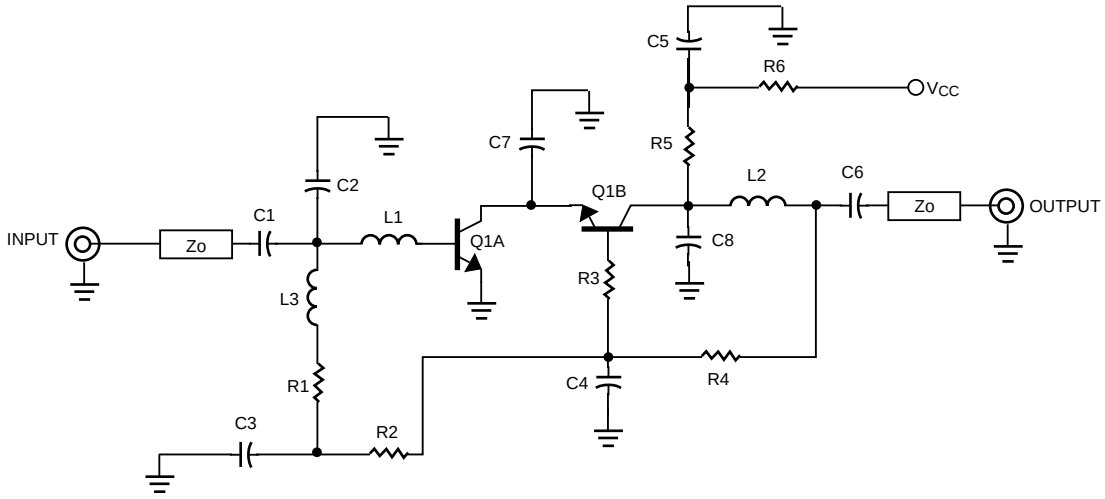
The input and output blocking capacitors and one of the bypass capacitors were increased in value for optimum operation at 300 MHz. In order to improve IP3 performance, R3 was decreased to 15 Ω and R5 increased to 1100 Ω. C8 and L2 were adjusted for a conjugate match.

Test Results

The performance of the prototype amplifier board is shown in tabular form in Table 4. Each device is biased at a V_{ce} of 1 volt and I_c of 600 µA. Input and output return loss in addition to gain are plotted in Figure 5.

The amplifier delivers its best output return loss of -22.7 dB at a frequency of 313 MHz. Since the output impedance of Q1B is very high, i.e. several thousand ohms, the output match is determined primarily by the shunt 1 pF capacitor and the 120 nH series inductor which provides the impedance match from 50 Ω to the 1100 Ω load resistor (R5). Since R5 is the dominant output impedance to be matched, the exercise of matching the amplifier to 50 Ω is very simple and can be done without knowledge of the device S parameters.

The input VSWR is very dependent on bias conditions. The input match will have to trade off gain, noise figure, and input match. Initially the frequency at which best noise figure and best input



C1, C6 = 100 pF CHIP CAPACITOR
C2 = 0-2 pF CHIP CAPACITOR (ADJ FOR NF/VSWR), C2 = 0 DEMO PCB
C3, C4, C5 = 1000 pF CHIP CAPACITOR
C7 = 0-2 pF (TRADE IP3 FOR NF), C7 = 0 pF DEMO PCB
C8 = 1 pF CHIP CAPACITOR
L1 = 82 nH CHIP INDUCTOR (COILCRAFT 1008CS-820)
L2 = 120 nH CHIP INDUCTOR (COILCRAFT 1008CS-121)
L3 = 330 nH CHIP INDUCTOR (COILCRAFT 1008CS-331)
Q1 = HEWLETT-PACKARD AT-32063 DUAL SILICON BIPOLAR TRANSISTOR
R1 = 50 OHM CHIP RESISTOR
R2 = 330K OHM CHIP RESISTOR (ADJUST FOR RATED I_C)
R3 = 15 OHM CHIP RESISTOR
R4 = 47 K OHM CHIP RESISTOR
R5 = 1.1 K OHM CHIP RESISTOR
R6 = OPTIONAL RESISTOR DEPENDING ON SUPPLY VOLTAGE (SEE TEXT)
Zo = 50 OHM MICROSTRIPLINE

Figure 4. Schematic Diagram and Parts List for AT-32063 300 MHz amplifier

Table 4. AT-32063 Amplifier Performance
$V_{ce1} = V_{ce2} = 1$ V and $I_c = 600$ µA

Freq. (MHz)	Gain (dB)	Noise Figure (dB)
300	21.6	1.22
310	21.9	1.18
320	21.6	1.18
330	21.0	1.15
340	20.5	1.15
350	19.3	1.20
360	17.4	1.24
370	15.3	1.29
380	13.6	1.33
390	12.4	1.45

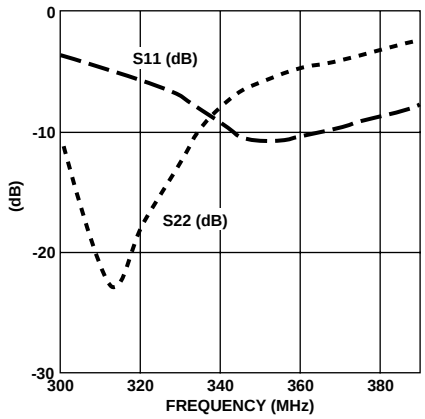


Figure 5. Swept Performance of 320 MHz Amplifier

return loss occurred did not occur at the same frequency. However, the final output matching capacitor used a shunt 1 pF capacitor at the collector of Q2 which actually improved input return loss also. Without the 1 pF capacitor, the best input return loss was only 4 to 5 dB.

Because of the resistive loading in the output stage, the resultant P1dB and IP3 were not as high as originally hoped. P1dB was measured at -16 dBm referenced to the output at 320 MHz. IP3 was measured by inserting two signals at 315 and 325 MHz into the amplifier. Output IP3 was found to be -3 dBm. This could be improved by adding up to several pF of capacitance to ground at the junction of the collector of Q1A and the emitter of Q1B. 4 pF improved the output IP3 to -2 dBm. Further improvement could be obtained by increasing the value of resistor R5 above 1.1K Ω. The drawback of increasing R5 would be that stability will be sacrificed and gain would also increase. The increase in gain may offset the improvement in output IP3 resulting in no improvement to input IP3.

300 MHz Amplifier No. 2 Circuit Design

The 300 MHz amplifier described in the previous section utilized resistive loading in both the base of Q1B as well as resistive loading in the collector circuit of Q1B. According to the Touchstone simulation, this was required to obtain unconditional stability through 4 GHz. The drawbacks of using resistive loading include reduced gain and output power capability. Since the resistive loading is not used at the input to Q1A, noise figure is impacted minimally. The additional disadvantage is that a 1100 Ω resistor in series with the power supply raises the power supply voltage required by the voltage drop across this resistor. The second 300 MHz amplifier is designed for operation from a 1 Volt power supply with a total collector current of only 600 µA.

Circuit Changes

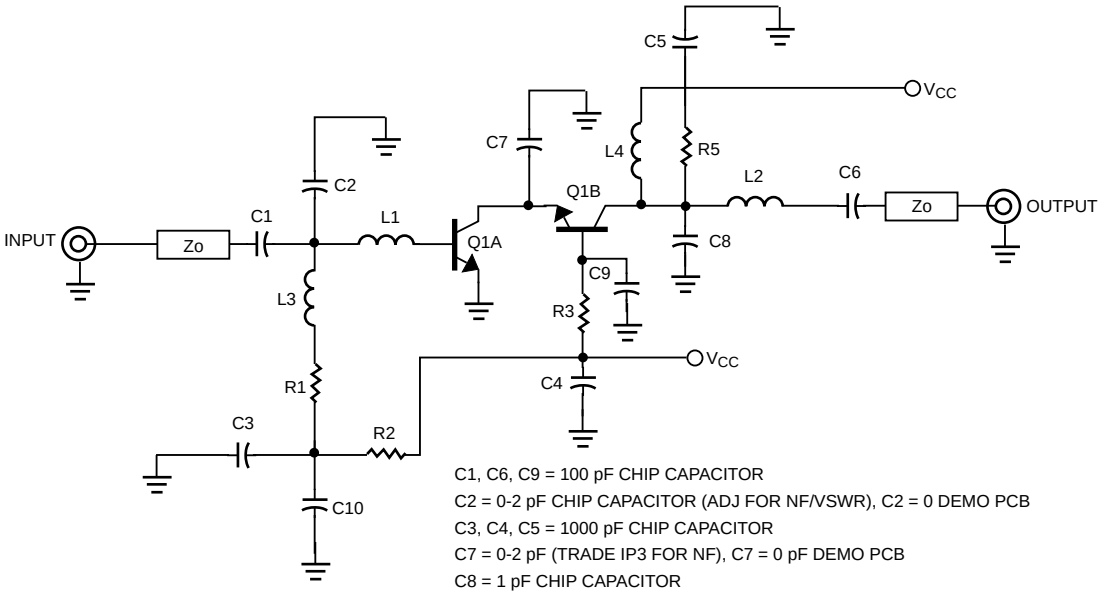
The schematic diagram and parts list for the modified 300 MHz amplifier is shown in Figure 6. The value of the output collector resistor, R5, is increased from 1100 Ω to 4700 Ω. R5 is then shunted with a 330 nH inductor similar to L3. The inductor in parallel with R5 serves 2 purposes. First, shunting the inductor across R5 reduces the dc voltage drop to 0 volts providing the full power supply voltage to the collector of Q1B. Second, the parallel combination of R5 and the inductor provides a good compromise between power output and stability. The base of Q1B is then bypassed with a 100 pF capacitor. Initial tests indicate that stability is still very good with no oscillations noticed.

Test Results

The results of the modified 300 MHz amplifier are shown in Table 5, page 6.

The modified AT-32063 Amplifier is biased at an I_c of 600 µA with a first stage V_{ce} of 0.36 V and a second stage V_{ce} of 0.64 V. The higher V_{ce} in the second stage was thought to improve IP3. The performance of the modified amplifier was very good.

It is interesting to note that highest output IP3 and best output return



C1, C6, C9 = 100 pF CHIP CAPACITOR
C2 = 0-2 pF CHIP CAPACITOR (ADJ FOR NF/VSWR), C2 = 0 DEMO PCB
C3, C4, C5 = 1000 pF CHIP CAPACITOR
C7 = 0-2 pF (TRADE IP3 FOR NF), C7 = 0 pF DEMO PCB
C8 = 1 pF CHIP CAPACITOR
C10 = 0.02 µF
L1 = 82 nH CHIP INDUCTOR (COILCRAFT 1008CS-820)
L2 = 120 nH CHIP INDUCTOR (COILCRAFT 1008CS-121)
L3, L4 = 330 nH CHIP INDUCTOR (COILCRAFT 1008CS-331)
Q1 = HEWLETT-PACKARD AT-32063 DUAL SILICON BIPOLAR TRANSISTOR
R1 = 50 OHM CHIP RESISTOR
R2 = 72.5 K OHM CHIP RESISTOR (ADJUST FOR RATED I_C)
R3 = 10 OHM CHIP RESISTOR
R4 = NOT USED
R5 = 4.7 K OHM CHIP RESISTOR
Zo = 50 OHM MICROSTRIPLINE

Figure 6. Schematic Diagram and Parts List for the modified 300 MHz amplifier

Table 5. Modified AT-32063 300 MHz Amplifier
V_{ce1} = 0.36 V, V_{ce2} = 0.64 V, I_C = 600 µA

Freq (MHz)	Gain (dB)	Noise Figure (dB)	S11 (dB)	S22 (dB)	Output IP3 (dBm)	Input IP3 (dBm)
250	15.0	1.40	-3.3	<-1		
260	16.6	1.30	-4.4	<-1		
270	19.0	1.29	-5.4	<-1		
280	21.7	1.23	-5.8	-1.2		
290	23.6	1.26	-5.7	-18.0	-3.7	-27.3
300	25.1	1.16	-6.0	-13.4	-2.5	-27.6
310	26.1	1.26	-6.2	-8.4	-1.8	-27.9
320	24.5	1.18	-5.6	-5.2	-0.7	-25.2
330	22.3	1.20	-4.7	-3.0	-0.6	-22.9
340	20.5	1.22	-4.1	-1.7	+1.3	-19.2
350	17.7	1.40	-3.5	<-1		

loss did not occur at the same frequency. It is a well known fact that a power match is different than a conjugate or gain match and some compromises may be necessary. The data suggests that the best power match produces an output return loss less than 2 dB. Best input match does coincide with minimum noise figure. However, attempting to improve input match at the expense of noise figure will cause gain to increase which will cause input intercept point to worsen. To a lesser but still somewhat significant level , the output match does effect input match as mentioned in the previous section.

Artwork

The artwork for a general purpose demonstration board is shown in Appendix B. Although the original artwork indicates a frequency of 850 MHz, the artwork and resultant circuit board provides a generic cascode circuit whose frequency of operation is determined by the proper choice of passive components. Actual component layout for the demonstration board is shown in Figure 7. The amplifier was designed to be etched on 0.062 inch FR-4/G-10 epoxy glass material.

Several circuit board changes are required for the original demonstration board. First, the input etched microstripline inductor should be removed and replaced with resistor R1. Inductor L1 attaches to resistor R1 and the input microstripline. A ground pad will have to be installed so that the new capacitor C8 which attaches to the collector of Q2 can be grounded. In a similar fashion, a new ground pad is required to install capacitor C7, if required.

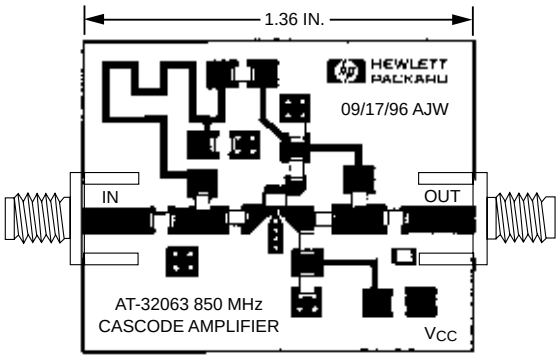


Figure 7. Original Demonstration board for AT-32063

Conclusion

The AT-32063 in a cascode configuration can provide less than a 1.2 dB noise figure, greater than 20 dB gain , and an output intercept point of +1.3 dBm at 340 MHz with only 600 µA of collector current from a 1 Volt power supply. At 850 MHz, the AT-32063 provides a nominal 1.3 dB noise figure and 18 dB gain at a bias current of 2 mA. Output intercept point of +6 dBm is achieved.

Appendix A

```
!AT-32063 850 MHz CASCODE LOW NOISE AMPLIFIER
!A.J.WARD 09-17-96

DIM
        FREQ    GHZ
        IND     NH
        CAP     PF
        LNG     IN

VAR

        C1#.1  2.24448  4       !INPUT SHUNT CAPACITOR,TRADE NOISE
                                !FIGURE/INPUT VSWR

        LL1=0.01                !Q1A EMITTER LEAD LENGTH, MAY BE ABLE TO TRADE OFF
                                !NOISE FIGURE, GAIN, STABILITY
        LL2=0.01                !Q1B EMITTER LEAD LENGTH, KEEP THIS AS SHORT AS
                                !POSSIBLE

CKT
        MSUB            ER=4.8          H=.062  T=.0014  RHO=1  RGH=0
        TAND            TAND=.002
        MLIN            1       2       W=.1  L=.05
        SLC             2       3       L=.25 C#0.5  15.7792  20 !INPUT BLOCKING CAPACITOR
        MLIN            3       4       W=.1  L=.2
        SLC             4       5       L=.25  C^C1     !SHUNT CAPACITOR, NOT USED IN DEMO
        VIA             5       0       D1=.03  D2=.03  H=.062  T=.0014
        IND             4       16      L#0  15  30
        RES             4       10      R=50    !PROVIDES LOW FREQUENCY STABILITY
        MLIN            10      11      W=.1  L=.1
        MSTEP           11      12      W1=.1  W2=.03
        MLIN            12      13      W=.03  L=1.5  !COULD BE REPLACED WITH WOUND
                                                !INDUCTOR
        SLC             13      14      L=.4 C=1000
        VIA             14      0       D1=.03  D2=.03  H=.062  T=.0014
        MLIN            16      17      W=.1   L=.1
        MSTEP           17      18      W1=.1  W2=.02
        MLIN            18      19      W=.02  L=.01
        DEF2P           1       19      INPUT

        S2PA            1       2  3    C:\S_DATA\BJT\T320631A.S2P   !COMMON EMITTER
                                                                     ! STAGE
        MLIN            3       4       W=.02   L^LL1
        VIA             4        0      D1=.030  D2=.030  H=.062  T=.001
        DEF2P           1       2       DEVICE1

        S2PB            1       2 3     C:\S_DATA\BJT\T320631A.S2P   !COMMON BASE STAGE
        MLIN            1       7       W=.02  L^LL2
        RES             7       8       R=50
        SLC             8       9       L=.25  C=100
        VIA             9       0       D1=.030  D2=.030  H=.062  T=.001
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```
        DEF2P       3       2       DEVICE2
        MLIN        1       2       W=.02 L=.030
        MSTEP       2       3       W1=.02  W2=.1
        MLIN        3       4       W=.1  L=.1
        RES         4       5       R=360   !PROVIDES LOADING FOR COMMON BASE STAGE
        MLIN        5       6       W=.1  L=.1
        SLC         6       7       L=.4  C=1000
        VIA         7       0       D1=.03  D2=.03  H=.062  T=.0014
        IND         4       20      L=33        !OUTPUT SERIES INDUCTOR
        SLC         20      21      L=.25  C=22   !OUTPUT BLOCKING CAPACITOR
        DEF2P       1       21      OUTPUT

        INPUT       1       2
        DEVICE1     2       3
        DEVICE2     3       4
        OUTPUT      4       5
        DEF2P       1       5       AMP

FREQ
        SWEEP       .1      1       .05
        SWEEP       1       6       .1

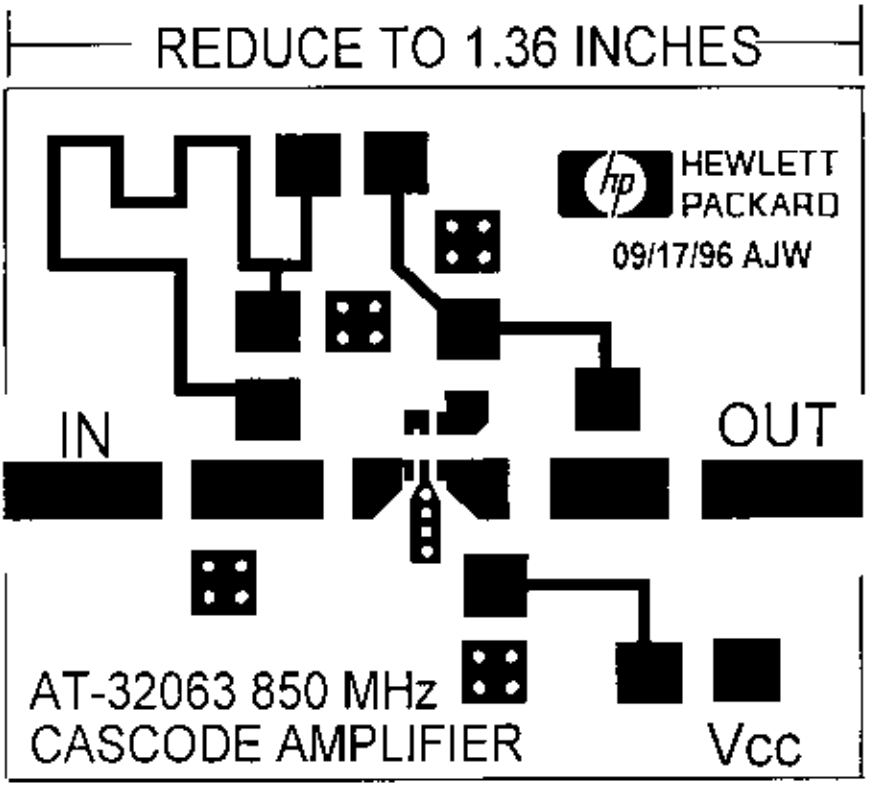
OUT
        AMP   DB[S11]
        AMP   DB[S21]
        AMP   DB[S12]
        AMP   DB[S22]
        AMP   NF
        AMP   K
        AMP   B1

OPT
        AMP  NF<1.5
```

FREQ-GHZ AMP	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1
0.10000	-3.254	1.727	-80.584	-2.264	125.335	939.410	0.598
0.15000	-6.025	3.927	-71.676	-2.347	117.822	382.289	0.522
0.20000	-8.379	5.358	-65.310	-2.405	112.100	180.668	0.487
0.25000	-9.108	6.547	-60.187	-2.464	10.765	91.112	0.487
0.30000	-8.093	7.657	-55.780	-2.530	7.196	47.238	0.512
0.35000	-6.508	8.735	-51.848	-2.607	5.441	24.734	0.557
0.40000	-5.065	9.786	-48.262	-2.698	4.367	12.997	0.616
0.45000	-3.951	10.807	-44.950	-2.809	3.624	6.889	0.682
0.50000	-3.180	11.798	-41.856	-2.951	3.065	3.757	0.750
0.55000	-2.895	12.592	-39.646	-3.168	2.621	2.597	0.805
0.60000	-2.918	13.361	-37.511	-3.480	2.260	2.024	0.851
0.65000	-3.215	14.130	-35.417	-3.944	1.971	1.747	0.892
0.70000	-3.735	14.911	-33.344	-4.678	1.758	1.597	0.936
0.75000	-4.340	15.678	-31.311	-5.936	1.624	.483	1.000
0.80000	-4.665	16.323	-29.423	-8.361	1.516	1.361	1.106
0.85000	-4.203	16.594	-27.923	-14.109	1.491	1.222	1.259
0.90000	-3.096	16.128	-27.171	-24.791	1.547	1.075	1.390
0.95000	-2.288	14.674	-27.578	-10.948	1.708	1.030	1.373
1.00000	-1.820	12.560	-28.638	-6.570	2.073	1.015	1.240
1.10000	-1.535	8.011	-31.681	-3.034	4.290	1.063	0.866
1.20000	-1.576	3.041	-35.114	-1.553	13.318	1.476	0.528
1.30000	-1.705	-1.923	-38.496	-0.830	114.803	2.407	0.302
1.40000	-1.895	-6.726	-41.655	-0.461	119.328	4.006	0.171
1.50000	-2.140	-11.319	-44.523	-0.268	122.744	6.519	0.099
1.60000	-2.442	-15.236	-47.129	-0.171	124.451	10.178	0.062
1.70000	-2.800	-18.923	-49.423	-0.116	124.727	15.635	0.041
1.80000	-3.226	-22.360	-51.372	-0.085	122.693	24.005	0.029
1.90000	-3.722	-25.231	-52.883	-0.065	23.049	33.741	0.021
2.00000	-4.240	-27.654	-53.855	-0.054	130.031	44.855	0.017
2.10000	-4.544	-29.625	-54.292	-0.045	134.683	52.125	0.014
2.20000	-4.133	-31.299	-54.324	-0.041	134.077	54.147	0.013
2.30000	-2.884	-33.100	-54.371	-0.039	137.611	50.310	0.014
2.40000	-1.552	-35.433	-54.831	-0.038	148.270	42.375	0.015
2.50000	-0.693	-37.983	-55.628	-0.038	162.421	30.071	0.016
2.60000	-0.274	-40.824	-56.664	-0.038	175.015	19.320	0.017
2.70000	-0.104	-43.748	-57.749	-0.038	185.632	11.886	0.017
2.80000	-0.052	-46.632	-58.795	-0.038	194.882	9.612	0.017
2.90000	-0.051	-49.393	-59.780	-0.039	203.077	14.830	0.018
3.00000	-0.068	-51.941	-60.707	-0.039	210.238	30.178	0.018
3.10000	-0.090	-54.104	-61.493	-0.038	216.139	55.041	0.017
3.20000	-0.111	-55.944	-62.261	-0.038	220.929	89.516	0.017
3.30000	-0.127	-57.447	-63.026	-0.037	224.624	130.918	0.017
3.40000	-0.137	-58.661	-63.804	-0.037	227.402	175.814	0.017
3.50000	-0.142	-59.679	-64.611	-0.036	229.567	221.554	0.016
3.60000	-0.142	-60.605	-65.467	-0.036	230.000	266.772	0.016
3.70000	-0.135	-61.532	-66.400	-0.035	230.000	310.680	0.016
3.80000	-0.122	-62.549	-67.450	-0.035	230.000	351.867	0.016
3.90000	-0.102	-63.751	-68.688	-0.035	230.000	387.466	0.016
4.00000	-0.077	-65.283	-70.242	-0.034	230.000	415.420	0.016

FREQ-GHZ AMP	DB[S11] AMP	DB[S21] AMP	DB[S12] AMP	DB[S22] AMP	NF AMP	K AMP	B1
4.10000	-0.052	-67.583	-72.381	-0.034	230.000	456.210	0.015
4.20000	-0.032	-70.932	-75.583	-0.033	230.000	604.125	0.015
4.30000	-0.024	-76.765	-81.276	-0.033	230.000	1.7e+03	0.015
4.40000	-0.022	-110.964	-115.339	-0.033	230.000	999.900	0.015
4.50000	-0.024	-76.821	-81.063	-0.033	230.000	1.6e+03	0.015
4.60000	-0.024	-70.470	-74.580	-0.033	230.000	381.806	0.015
4.70000	-0.025	-66.610	-70.588	-0.034	230.000	160.643	0.015
4.80000	-0.027	-63.738	-67.583	-0.034	230.000	88.073	0.015
4.90000	-0.031	-61.405	-65.118	-0.034	224.139	59.159	0.016
5.00000	-0.040	-59.432	-63.013	-0.034	217.259	47.216	0.016
5.10000	-0.055	-57.746	-61.196	-0.034	210.837	42.835	0.016
5.20000	-0.079	-56.333	-59.652	-0.033	204.538	42.089	0.015
5.30000	-0.112	-55.206	-58.395	-0.031	197.927	43.240	0.014
5.40000	-0.158	-54.390	-57.449	-0.029	190.043	45.583	0.013
5.50000	-0.218	-53.897	-56.828	-0.025	175.876	48.991	0.011
5.60000	-0.290	-53.721	-56.524	-0.022	178.478	53.705	0.010
5.70000	-0.374	-53.831	-56.509	-0.019	184.885	60.200	0.008
5.80000	-0.460	-54.188	-56.741	-0.017	187.749	68.947	0.007
5.90000	-0.532	-54.746	-57.175	-0.015	189.833	79.872	0.007
6.00000	-0.566	-55.439	-57.747	-0.014	191.808	91.260	0.006

Appendix B



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