Phase Locked Loop Frequency Synthesizer Demonstration Circuit Board

Application Note 1145

Objective

This document details the evaluation procedures and usage of the Hewlett-Packard HPLL-8001 demonstration circuit board and evaluation software. All operating conditions and electrical characteristics of the HPLL-8001 are described in the current version of the data sheet.

Introduction

The evaluation materials were developed to enable customers to verify functionality and to test the performance of the HPLL-8001 synthesizer. This document also outlines how to use the component in a synthesizer loop for a GSM application. To evaluate the HPLL-8001 as described in this document, the following items are needed:

1) A PCB with a synthesizer loop using the HPLL-8001, a high frequency prescaler, a loop filter, and a VCO.

2) Software running under Windows to program the synthesizer loop. (Available on www.hp.com/go/rf).

3) This document.

PCB Description

Figure 1 illustrates the internal configuration of the synthesizer. The circuit diagram shown in Figure 2 details the schematics of the PLL frequency synthesizer PCB.

The high frequency portion of the demo circuit contains a 925 MHz center frequency VCO module. Its output power is typically around 3 dBm into 50 Ω. The RF signal is applied to a prescaler via a pad and a resistive divider.

The prescaler scales down the RF signal. Its dividing ratio P can be programmed over the software interface.

P = 32/33
P = 64/65
P = 128/129

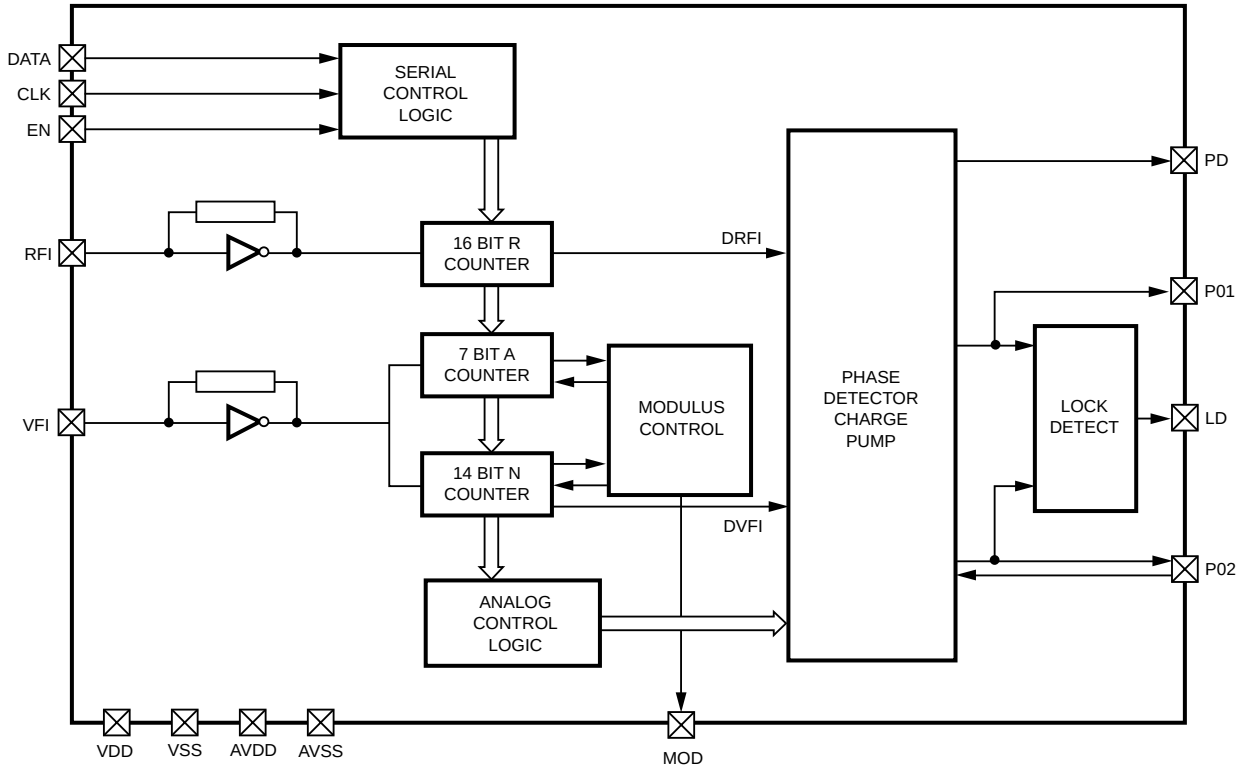

Figure 1. HPLL-8001 Internal Block diagam

The HPLL-8001 acts as a PLL controller. It contains the R-counter for scaling down the reference signal applied at port REF (SMC) connector, the N- and A-counters that divide the prescaler's output signal, the serial control logic (via a 3-wire bus), and the phase detector with charge pump. The following counter settings are possible:

A = 0 to 127
N = 3 to 16,380
R = 3 to 65,535

The reference signal, REF, covers the 1 to 70 MHz range with a minimum level of 100 mV_{rms}. The input REF is AC coupled. The loop filter, together with the phase detector output current (PD_OUT), defines the dynamic behavior of the PLL loop. The greater the time constant, the longer the switching time – but the better the suppression of the spurious signal. The value of the phase detector output current at PD_OUT defines the loop gain. Both parameters have to be calculated and chosen for each specific application.

All settings are made via the 3-wire control bus (data, clock, enable), therefore serial data are provided by a Sub-D-25 connector. The interface IC CD40109 separates the circuitry from the PC's printer port LPT1, and additionally performs the tristate for the RS pin. The easy-to-use software runs under Windows and controls all synthesizer functions. The VCO section and the ICs are powered separately with two different power supplies to prevent parasitic signal coupling through the V_{CC} rails.

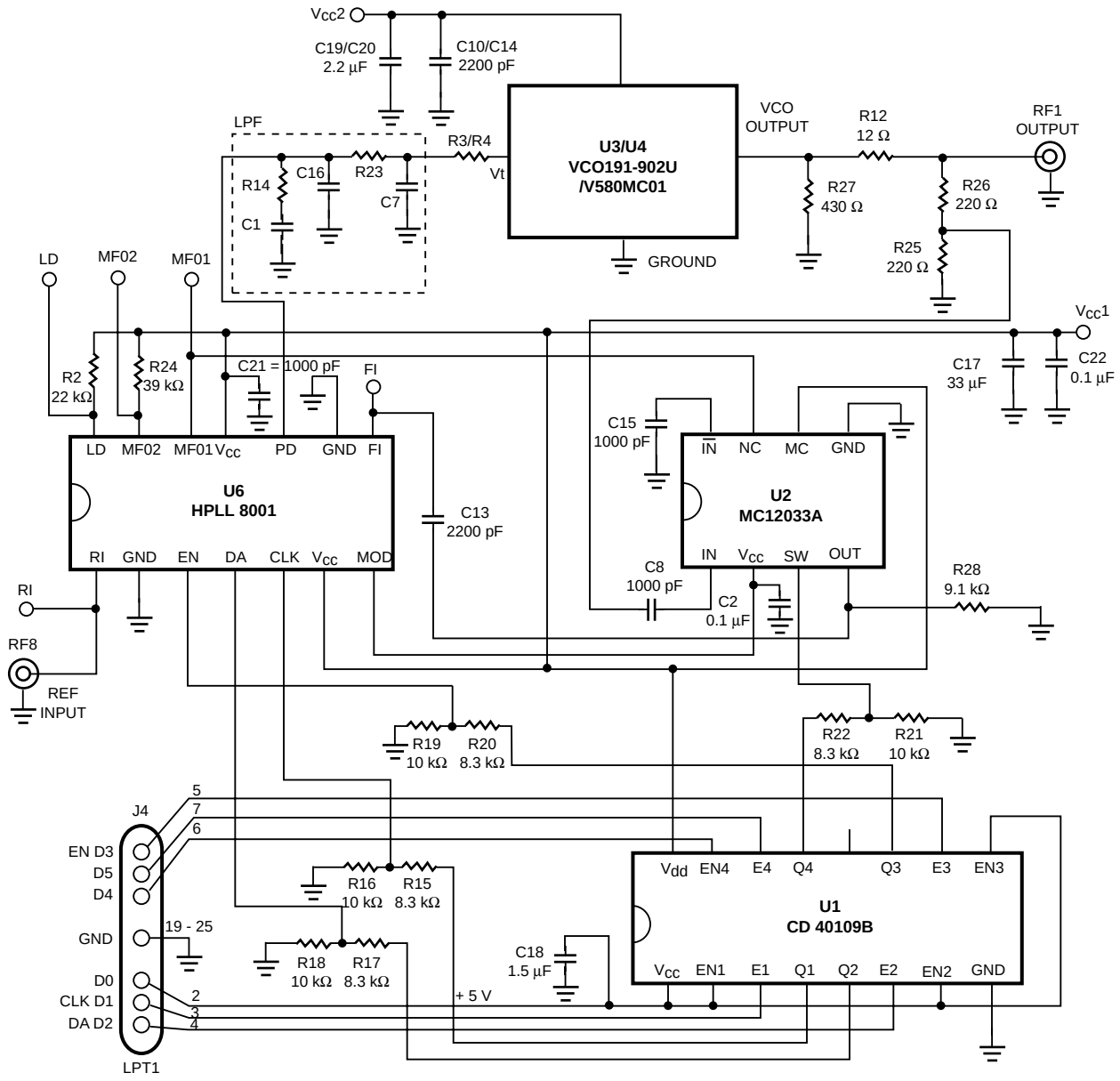

Figure 2. PLL Frequency Synthesizer Schematic

Software

The HPLL-8001 evaluation board can be programmed using software running under Microsoft Windows 3.1. The software includes the following files:*

hp8001.exe: the executable of the control program.
Readme.txt: latest information on the current release.
gsm_dual.ini: file with initial settings for a GSM application in dual mode.
gsm_sing.ini: file with initial settings for a GSM application in single mode.

* These files are located at www.hp.com/go/rf.

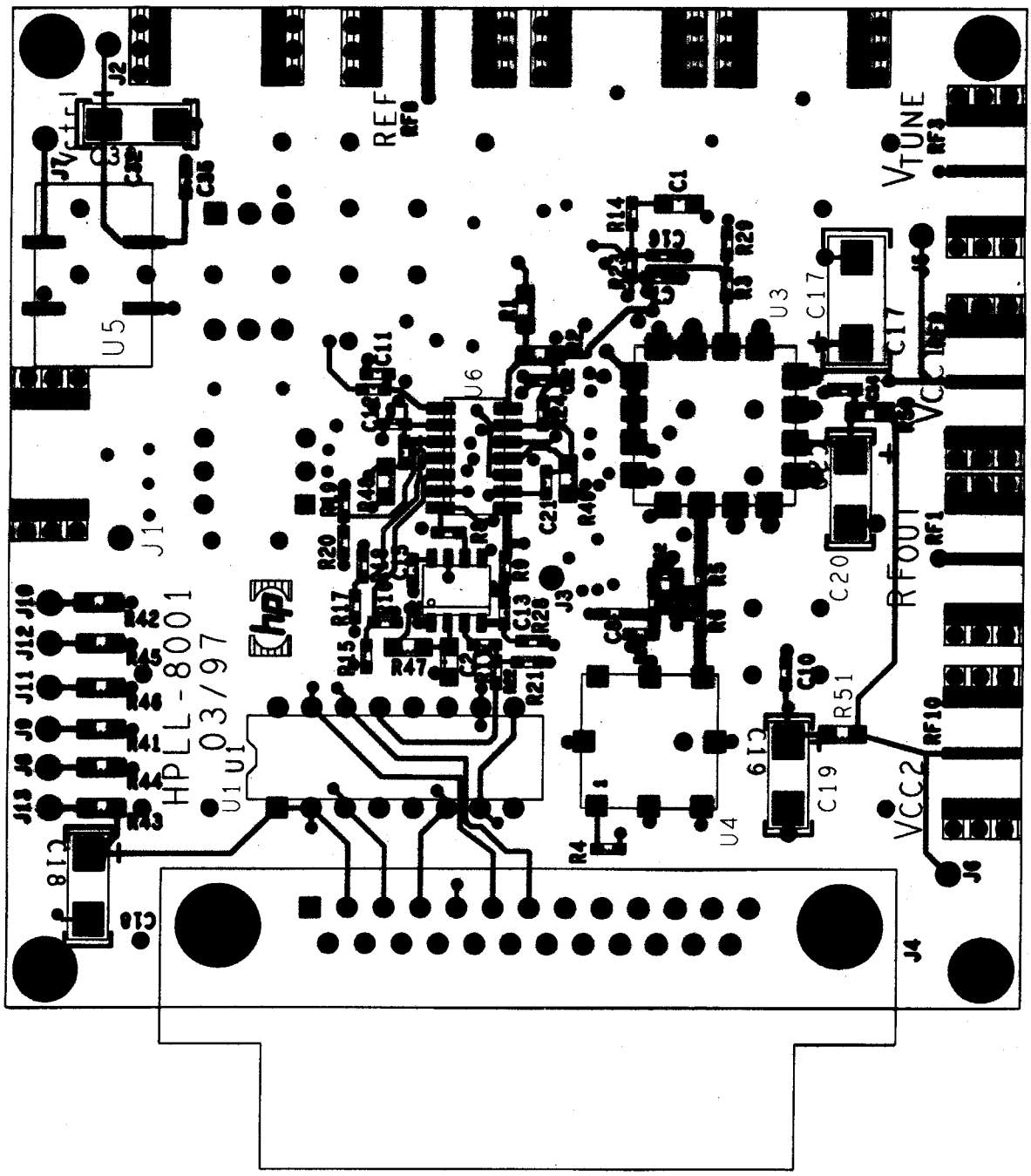

Figure 3. Demo Board PCB Layout

The required values for all programmable bits are selected by clicking on the appropriate variable until the correct value is displayed on the screen. The messages R counter, N and A counters, Status and the HPLL-8001 divider ratio are displayed on the bottom of the window and can be sent together or separately to the PCB. The selection between Status and Reduced Status is done at the top of the window. If Reduced Status is selected, the inappropriate variables are blanked. The selected data is transferred by clicking on the button “sent”.

Table 1. Demo Board Bill of Material.
Values shown are for GSM frequency range 890 - 960 MHz.

Board Designation	Description	Part Number	Function
U1	Voltage Level shifter	Harris CD 40109	Interface with PC parrallel port signals
U2	Prescaler	Motorola MC12033A	Dual modulus frequency divider
U3/U4	VCO	Varil 191-902U / Zcomm V580MC01	Voltage Controlled Oscillator
U5	X-tal Oscillator	Valpey Fisher VF954	Used as a 13 MHz reference source
U6	PLL Freq. Synth.	HP HPLL-8001	Device Under Test
C1, 7, 16	Loop filter caps.		Values depend on filter design
C10, 14	2200 pF		
C19, 20	2.2 µF		
C17	33 µF		Bypass capacitor
C21, 35	1000 pF		Bypass capacitor
C22	100 pF		Bypass capacitor
C18	1.5 µF		Bypass capacitor
C2	0.1 µF		Bypass capacitor
C13	2200 pF		AC coupling between prescaler and DUT
C32	1.5 µF		Bypass capacitor
C11,12	2200 pF		AC coupling between DUT and off- board or on-board reference source
C15	1000 pF		AC ground for the input_bar of the prescaler
R14, R23	Filter resistor		Values depend on filter design
J4	25 DB connector		
R3, 4, 5, 6, 11	0 Ω		Used as jumpers for different options
R12	12 Ω		VCO output attenuator
R27	430 Ω		VCO output attenuator
R25, 26	220 Ω		VCO output attenuator
R24	39 KΩ		
R2	22 KΩ		
R15, 17, 20, 22	8.3 KΩ		Voltage divider circuit from 5 V to 3 V
R16, 18, 19, 21	10 KΩ		Suggested by Motorola data sheet
R28	9.1 KΩ		Suggested by manufacturer
L6	jumper		To ground synthesizer digital ground

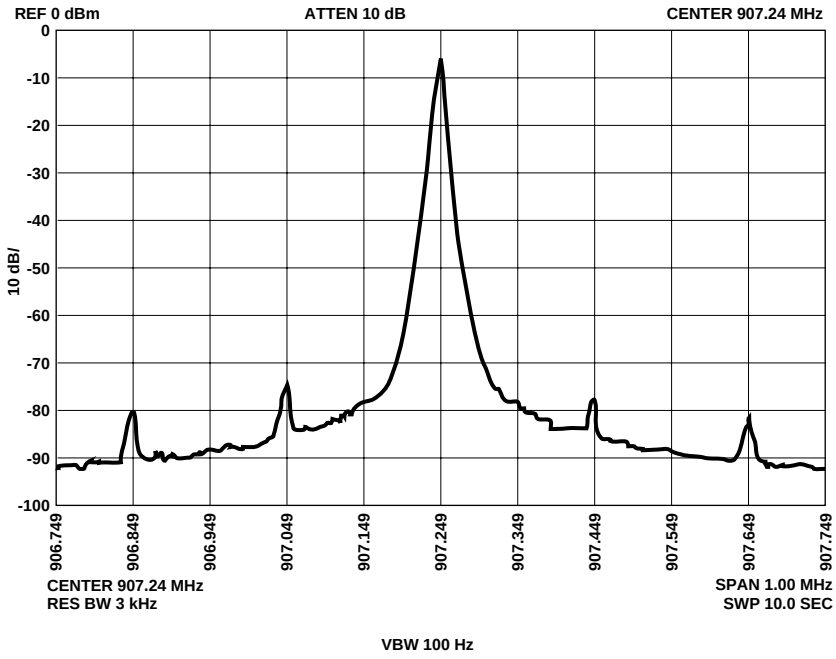

Figure 4. Typical GSM Spectrum Plot

www.hp.com/go/rf
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Data Subject to Change

5967-6012E (1/99)