800 to 950 MHz Amplifiers using the HBFP-0405 and HBFP-0420 Low Noise Silicon Bipolar Transistors

Application Note 1161

Introduction

Hewlett-Packard's HBFP-0405 and HBFP-0420 are high performance isolated collector silicon bipolar transistors housed in 4-lead SC-70 (SOT-343) surface mount plastic packages. Both the HBFP-0405 and HBFP-0420 are described in low noise amplifiers for use in the 800 to 950 MHz frequency range. The amplifiers are designed for use with 0.032 inch thickness FR-4 printed circuit board material. The HBFP-0405 amplifier is biased at a V_{ce} of 2 V and I_c of 5 mA and provides a 1.95 dB noise figure, 22 dB gain and an output intercept point of +15.5 dBm. The HBFP-0420 amplifier is biased at a V_{ce} of 2 V and I_c of 8 mA and provides a 1.35 dB noise figure, 20 dB gain and an output intercept point of +18 dBm.

HBFP-0405 LNA Design

The HBFP-0405 amplifier is designed for a V_{ce} of 2 volts and I_c of 5 mA. Typical power supply voltage, V_{cc}, would be in the 2.7 to 3 volt range. Higher V_{cc} will result in better bias point stability over temperature. For higher power supply voltages resistor R5 can be used to help set the collector voltage for a given collector current. The amplifier schematic is shown in Figure 1.

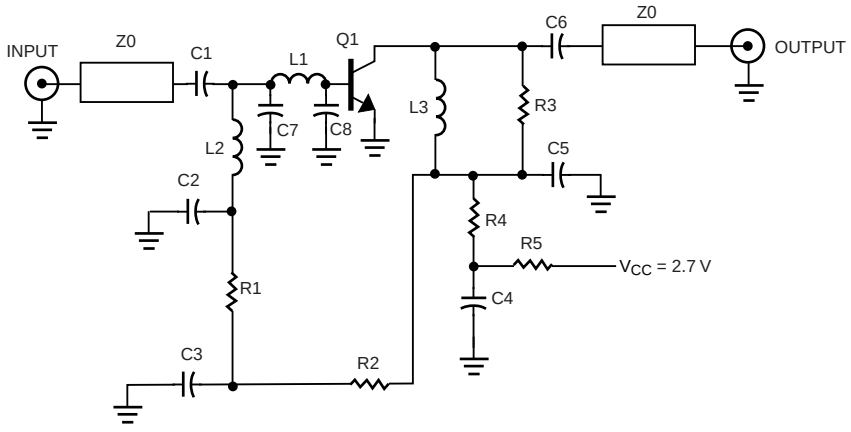

Figure 1. Schematic Diagram

The artwork and component placement drawing for the HBFP test board is shown in Figure 2. A component list is shown in Table 1.

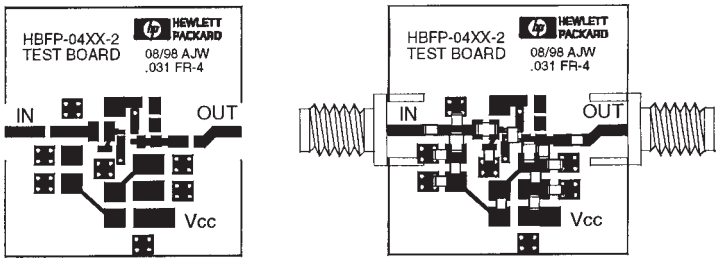

Figure 2. 1X Artwork and Component Placement Drawing

Table 1. Component Parts List

C1	1.8 pF chip capacitor
C2, C5	47 pF chip capacitor
C3, C4	1000 pF chip capacitor
C6	2.7 pF chip capacitor
C7	0.8 pF chip capacitor
C8	1.3 pF chip capacitor
L1	18 nH chip inductor (Coilcraft 1008CS-180)
L2	470 nH chip inductor (Coilcraft 1008CS-471)
L3	10 nH chip inductor (Coilcraft 1008CS-100)
Q1	Hewlett-Packard HBFP-0405 Silicon Bipolar Transistor
R1, R4	50 Ω chip resistor
R2	24 KΩ chip resistor (adjust for rated Ic)
R3	470 Ω chip resistor
R5	91 Ω chip resistor for Ic = 5 mA, Adjust for supply voltages other than Vcc of 2.7 Volts
Zo	50 Ω microstripline

The input match uses a three element low pass network consisting of L1, C7 and C8. The 3 element network provides a very good input return loss coincident with moderate noise figure. C1 provides a dc block and also provides some low frequency gain roll-off. L2, C2, R1 and C3 provide bias decoupling and a good low frequency termination for the device. The output impedance matching network is a high pass structure consisting of a series capacitor, C6, and a shunt inductor, L3. A resistor, R3, is paralleled across the shunt inductor to enhance broad band stability by lowering amplifier gain. C5, R4, and C4 provide bias decoupling and a low frequency resistive termination for the device. Surface mount Coilcraft inductors were chosen for their small size.

Performance of the HBFP-0405 at V_{ce} = 2 V and I_c = 5 mA

The HBFP-0405 amplifier has been designed for best input return loss, good output IP3 and reasonable output return loss. Obtaining a good input return loss along with a good output return loss requires some compromise in noise figure. According to the data sheet, the HBFP-

0405 has a 1.36 dB F_{min} at the specified bias conditions. Considering the losses associated with matching for optimum noise figure on a lossy FR-4 printed circuit board, the best noise figure that could be achieved in an actual amplifier is in the 1.5 to 1.6 dB range. With a match optimized solely for best noise figure, the best input return loss that could be expected would be 6 to 7 dB. The HBFP-0405 amplifier achieves a 1.95 dB noise figure while achieving greater than 15 dB input return loss. The measured noise figure and gain of the completed amplifier is shown in Figures 3 and 4. Noise figure is a maximum of 2.1 dB from 820 MHz to 920 MHz. Typical gain is greater than 20 dB from 800 MHz to 900 MHz. Input and output return loss is shown in Figure 5. The input return loss is greater than 10 dB from 835 to 900 MHz. The output return loss was measured at nearly 10 dB at 900 MHz.

There is considerable tuning interaction between the input and output matching networks in any single stage amplifier. Having a somewhat better input return loss coincident with low noise figure may necessitate a compromise in output return loss. The use of resistor R3 helps to isolate the input from the output and also provides broadband stability. A drawback of using resistive loading in the collector circuit is decreased power output.

Output intercept point, IP3, was measured at several frequencies from 850 MHz through 950 MHz. The best IP3 is +15.5 dBm and occurs between 900 and 950 MHz. IP3 at 850 MHz decreases to +14.8 dBm. The output return loss is relatively constant at 9 to 10 dB over the same frequency range. Output IP3 can be improved by approximately a dB by increasing the value of the stabilization resistor R3. Output return loss may get worse and stability will suffer.

HBFP-0420 LNA Design

The HBFP-0420 amplifier is designed for a V_{ce} of 2 volts and I_c of 8 mA. Typical power supply voltage, V_{cc}, would be in the 2.7 to 3 volt range. The HBFP-0420 amplifier uses the same demo board as described for the HBFP-0405. The schematic diagram for the HBFP-0420 amplifier is similar to the one for the HBFP-0405 shown in Figure 1. The main difference being that the capacitors C7 and C8 are not required but could be used for fine tuning noise figure and input return loss. A list of components is shown in Table 2.

The input matching network uses a series inductor for the noise match. Some fine tuning for lowest noise figure or improved input VSWR can be accomplished by adding capacitance to ground at either end of L1. C1 provides a dc block and also provides some low frequency gain roll-off. L2, C2, R1 and C3 provide bias decoupling and a good low frequency termination for the device. The output impedance matching network is a high pass structure consisting of a series capacitor, C6, and a shunt inductor, L3. A resistor, R3, is paralleled across the shunt inductor to enhance broadband stability by lowering amplifier gain. C5, R4, and C4 provide bias decoupling and a low frequency resistive termination for the device. Surface mount Coilcraft inductors were chosen for their small size.

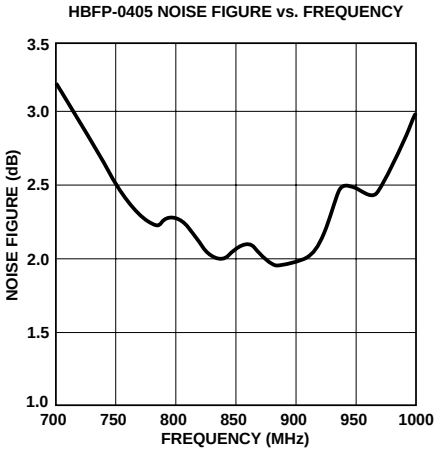

Figure 3. Noise Figure vs. Frequency.

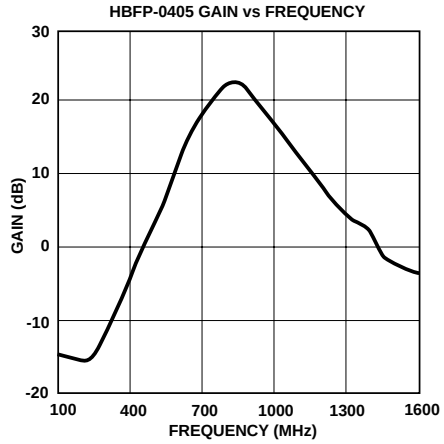

Figure 4. Gain vs. Frequency.

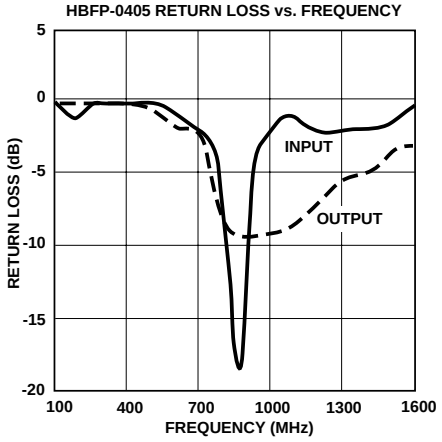

Figure 5. Input/Output Return Loss.

Table 2. Component Parts List.

C1	27 pF chip capacitor
C2, C5	47 pF chip capacitor
C3, C4	1000 pF chip capacitor
C6	3.6 pF chip capacitor
C7, C8	Not required but could be used for fine tuning noise figure and return loss
L1, L3	8.2 nH chip inductor (Coilcraft 0805CS-080XMBC)
L2	470 nH chip inductor (Coilcraft 1008CS-471)
Q1	Hewlett-Packard HBFP-0420 Silicon Bipolar Transistor
R1, R4	50 Ω chip resistor
R2	15 KΩ chip resistor (adjust for rated Ic)
R3	215 Ω chip resistor
R5	36 Ω chip resistor for Ic = 8 mA. Adjust for supply voltages other than Vcc of 2.7 Volts
Zo	50 Ω microstripline

Performance of the HBFP-0420 at V_{ce} = 2 V and I_c = 8 mA

The HBFP-0420 amplifier has been designed for best possible noise figure with a reasonable input return loss. As shown in Figure 6, the noise figure measured 1.35 dB between 800 and 850 MHz. Associated gain measured greater than 20 dB from 600 MHz through 950 MHz. A plot of gain versus frequency is shown in Figure 7. Input and output return loss is shown in Figure 8. The input return loss is 9 dB at 830 MHz. The output return loss measures greater than 10 dB from 650 through 925 MHz.

Output intercept point, IP3, was measured between 800 MHz and 950 MHz in 50 MHz increments. IP3 was then compared to output return loss as shown in Figure 9. The output IP3 measured +18 dBm from 850 through 950 MHz. IP3 could be improved slightly if resistor R3 were increased in value. However, gain will increase and stability may be sacrificed.

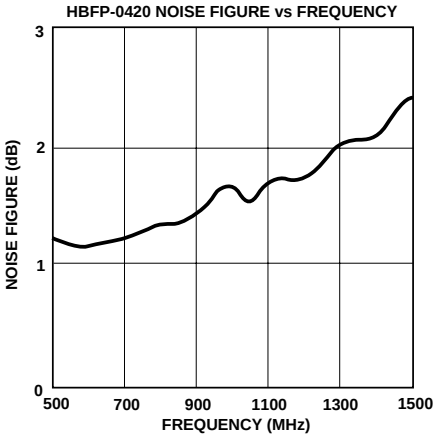

Figure 6. Noise Figure vs. Frequency

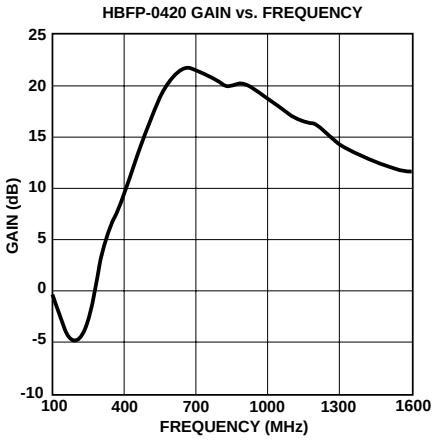

Figure 7. Gain vs. Frequency.

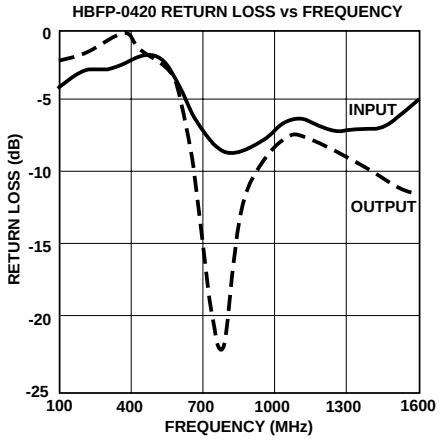

Figure 8. Input/Output Return Loss.

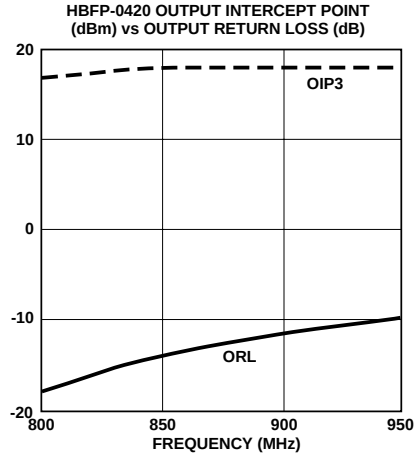

Figure 9. Output Intercept Point and Return Loss vs. Frequency.

Using the HBFP-04XX-2 Demo Board at Other Frequencies

The demo board and design techniques presented here can be used to build low noise amplifiers for other frequencies in the VHF through 1700 MHz frequency range. The input and output matching networks can be scaled for small frequency excursions with good success. For best success it is suggested that a careful circuit analysis be performed with the help of one of the linear circuit simulators such as those generated by HP/EEsof. The demo board also includes several extra pads that are routed from the collector to the base of the transistor. These experimental pads can be used to supply external shunt R/L/C feedback around the transistor for future designs.

Conclusion

Both the HBFP-0405 and HBFP-0420 can provide economical low noise, high gain and moderate IP3 LNA solutions for various commercial applications in the 800 to 950 MHz frequency range. Successful amplifier design is a careful balance between various parameters including noise figure, gain, return loss, intercept point and dc power availability.

Low Noise Amplifier Design Primer

Introduction

Successful low noise amplifier design requires careful circuit modeling and may involve some performance tradeoffs. As an example, designing an amplifier to achieve the best noise figure that the device is capable of along with its rated associated gain does not necessarily guarantee a very good input return loss or a very stable amplifier. Gain may have to be sacrificed to enhance stability. Gain and or noise figure may also have to be traded off for improved input return loss. These and other tradeoffs must be carefully evaluated.

Evaluation of S Parameters

The first step to successful amplifier design is to evaluate the device S Parameters. In a common emitter configuration, a 50 Ω source will be connected to the base of the transistor and a 50 Ω load will be connected to the collector of the transistor. The common lead or emitter(s) will be connected to ground. This is equivalent to evaluating the device without external matching networks. Calculating the Rollett Stability Factor K from the four S Parameters at each frequency will give insight into the device's stability. At frequencies where K is greater than or equal to 1, the device is unconditionally stable regardless of input or output terminations. When $K < 1$, the device is conditionally stable indicating that certain input or output terminations may cause the device to be unstable. An amplifier that is not unconditionally stable may still be a useful amplifier provided that stability circles for both the input and output planes are calculated. It is then a simple matter of ensuring that certain undesired impedances are not presented to the device.

As with most discrete transistors, the device will not be unconditionally stable at all frequencies. Making a device unconditionally stable or as near unconditionally stable as possible over a wide frequency range is the challenge left to the circuit designer. Certain techniques such as emitter degeneration and resistive loading can be used to enhance stability. These topics will be discussed in the following sections.

Device Grounding

The entire stability picture changes when the device is mounted on a microstrip circuit board. The device is elevated above electrical ground by placing the device on the top side of the microstrip board and using plated through holes to attach each emitter lead to ground. However short the 0.031 inch or 0.062 inch long plated through holes may appear, the plated through holes can add significant inductance in series with the device. The old "school of thought" of thinking that the device common leads need to be "hard grounded" to get performance out of a discrete transistor does not apply to all transistors. High frequency PHEMT devices generally require very good grounds because of their very small geometry and very high frequency gain. Most bipolar devices are more tolerant of greater inductance in series with the emitter grounding. Actually, some degree of equivalent

inductance in series with the emitter leads can actually improve overall amplifier performance. The effect of the emitter inductance is best analyzed with the help of a good microwave circuit simulator such as those created by HP EEsof.

In order to remedy the modeling difficulty associated with adding the model for the plated through holes and modeling the complex union between the device leads and the plated through hole grounds, the device S and Noise Parameters can on occasion include the effect of device grounding. Such is the case with the Hewlett-Packard HBFP series of low noise silicon bipolar transistors. The S and Noise Parameters for the HBFP series of transistors are measured on a microstripline made on a 0.025 inch thickness alumina carrier. The input reference plane is at the end of the base lead. The output reference plane is at the end of the collector lead. The S and Noise parameters include the effect of four plated through holes connecting the emitter leads on the top side of the board to the microstrip groundplane on the bottom side of the carrier. Two 0.020 inch diameter holes are placed within 0.010 inch from each emitter lead contact point with one via on either side of that point.

Effect of Emitter Inductance

The cross sectional view of a transistor with two emitter leads connected to the bottom side groundplane with the use of plated through holes is shown in Figure 10. The distance LL is 0.0 when the device S and Noise Parameters are measured. Adding additional inductance in the form of top-side etch, shown as additional distance LL, can be used to improve in-band stability and input return loss.

The graph in Figure 11 shows the effect of emitter lead length (LL) on stability factor versus frequency for the Hewlett-Packard HBFP-0420. The HBFP-0420 is biased at a Vce of 2 volts and and Ic of 5 mA. The additional microstrip etch has a width of 0.040" and is varied from zero to 0.12" in length. Length LL is measured from the edge of the plated through hole to the edge of the emitter lead.

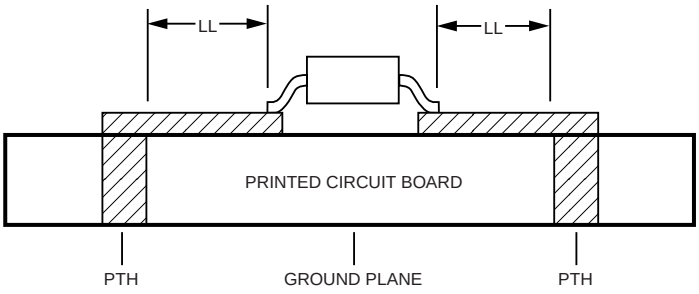

Figure 10. Cross-sectional View Showing Emitter Connections to Groundplane.

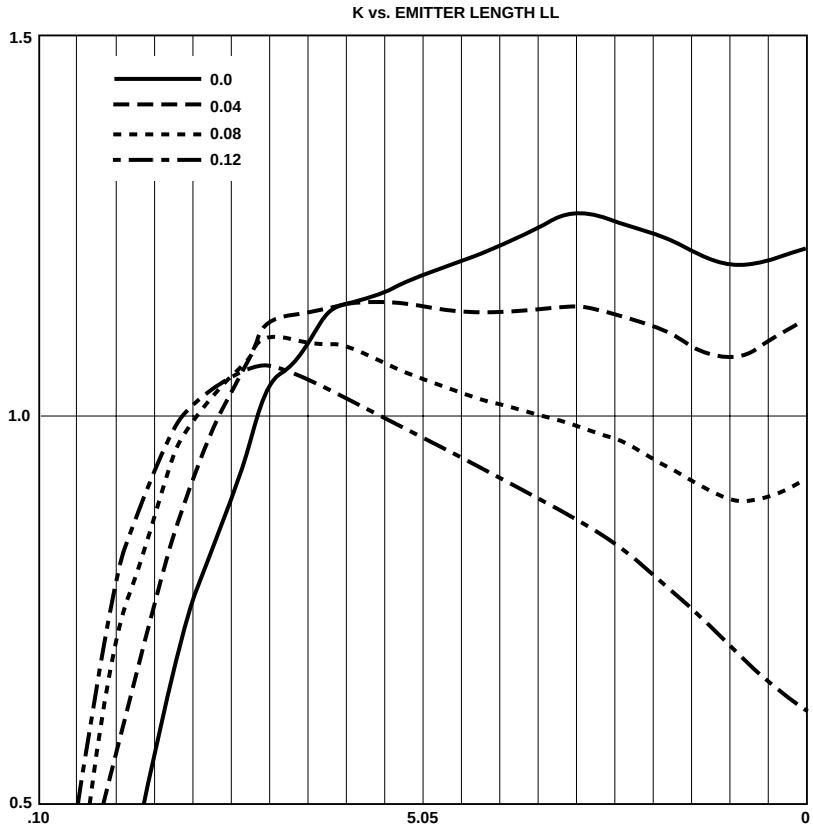

Figure 11. Stability Factor vs. Emitter Lead Length LL.

With minimal value of LL, the device exhibits very good high frequency (near 10 GHz) stability as evidenced by K being greater than 1. As LL is increased in 0.040" increments, one observes that K improves at lower frequencies and becomes worse at higher frequencies. At the lower frequencies below 2 GHz where K is less than 1, the additional emitter inductance is used to increase K above 1 if possible. The limitation on how much additional emitter inductance can be used depends on what effect the additional inductance has on stability at higher frequencies. As can be seen from Figure 11, excessive values of LL can produce greater potential for high frequency oscillations.

For the HBFP-0420, a value of 0.080" was used as a starting value for LL. Once the matching networks are attached to the device, some fine-tuning of this value may be in order. Using emitter inductance to improve stability at lower frequencies where the device is actually going to be operated is a fairly lossless method of stabilization. Lossless means that noise figure and power output are minimally effected. Generally some in-band gain is sacrificed to enhance stability but this will also improve input intercept point. Another very important aspect of emitter inductance is its ability to improve input return loss without sacrificing noise figure. The addition of inductance in series with the emitter has the effect of forcing S11* and Γo (reflection coefficient required for best noise figure) closer in value. Therefore,

the best input return loss and lowest noise figure have a better chance of occurring simultaneously.

When modeling the additional emitter lead length, keep in mind that the circuit simulators generally assume that the emitter is a single node. Therefore, when adding additional emitter lead length in the form of LL, it should be simulated as two microstriplines in parallel of width W and length LL in series with the transistor common lead and ground. In the case of the HBFP transistors, adding additional emitter lead length LL appears to be in series with the bottom of the plated through hole and ground. Its effect is the same as placing it between the emitter and the top side of the plated through hole.

Impedance Matching Networks

Impedance matching networks can take on any of several different configurations based on frequency and space allocations. A low loss matching network with good bandwidth at 900 MHz would be a low pass topology consisting of a series inductor. Shunt capacitance on either side of the series inductor could be used for fine tuning. A shunt inductor which would be used for bias decoupling also acts as a high pass filter for low frequency rejection. Choosing a small value dc blocking capacitor also aids in reducing low frequency gain. A simple output matching network could consist of a shunt inductor/series capacitor in a high pass topology. Again, the shunt inductor also provides a means of injecting collector voltage. A small value dc blocking capacitor also provides low frequency gain reduction.

Once a rough check is performed to determine the optimum circuit configuration for both the noise matching circuit on the input and the gain match circuit on the output, the computer can be used to optimize performance. With the input optimized for best noise figure and output optimized for best associated gain (G_a), other amplifier parameters start to unfold. Most notable may be that the circuit is not unconditionally stable and the input return loss is not very good.

Designing an amplifier to produce G_a (Associated gain at minimum noise figure) may not necessarily guarantee unconditional stability. One may find that a dB or two of gain may have to be sacrificed to enhance stability. There are several ways to accomplish this gain reduction. Designing the output circuit for an intentional mismatch is one way to lower gain which will enhance stability. Unfortunately, the intentional mismatch results in a high output VSWR which could add passband ripple, especially if a filter is to be cascaded with the amplifier.

Lossless feedback in the form of emitter inductance is quite often the first item to optimize. Take a second look at the effect that emitter inductance has on overall stability from 100 MHz to 10 GHz. Consider a re-adjustment from the earlier value that was picked based on just the S Parameters. As discussed in an earlier section, a small amount of emitter inductance can be used to reduce gain, enhance stability and even improve input return loss. The use of emitter inductance is a

powerful tool if used properly. Be cautious about adding an excessive amount of emitter inductance. Make sure that the amplifier circuit is analyzed for stability from as low as 100 MHz to as high frequency as the device has S Parameters. Although it might appear from the computer simulation that adding considerable emitter inductance will make the amplifier circuit unconditionally stable in-band (i.e., at 900 or 1900 MHz), excessive inductance may have actually created a potential instability at a much higher frequency. The emitter inductance has a degenerative effect at lower frequencies and a regenerative effect at higher frequencies.

After determining the appropriate amount of emitter inductance, the task of stabilization can be best accomplished with the use of resistive terminations. Theoretically, resistive loading can be used in series with the emitter, base, or collector port or in shunt with any 2 ports. In a typical low noise amplifier in a common emitter configuration, it is generally desirable to minimize the use of resistive loading in the emitter and base ports of the device. Any shunt resistive loading that includes the base port will also add to the noise figure unless some reactive components are used in series with the resistive loading to minimize its effect at a particular frequency. The best place to use resistive loading would then be the collector. The resistive loading can be in series with the collector or in shunt between the collector and ground. Ground is defined as the common return point for all 3 device terminals. This is generally the bottom groundplane in a typical microstrip layout and not the emitter pad(s). Remember that the emitter is elevated above the groundplane by virtue of the plated through hole(s) and any associated lead length.

The use of a resistor in series with the collector does provide a convenient broadband de-Qing element which does enhance stability. Shunt resistive loading is a convenient way to provide a broadband termination for an otherwise high impedance device. Lowering the resistor value tends to swamp out the loading effect of the transistor making the device very stable over a very wide frequency range. A simple 2 element matching network can then provide a very good output VSWR. The undesirable side effect is some loss of gain but most notable output P1dB and IP3. P1dB and IP3 may have to be traded off for stability and output return loss. Other techniques such as lossless feedback and feedforward techniques can be used to improve IP3. They require an increase in component count and real estate and are beyond the scope of this application note.

It is important to note that even though some transistors may have higher G_a and higher S21, the key parameter would be how much stable gain can be achieved from a particular amplifier design. High amplifier gain is useless if the amplifier is sensitive to terminations. Most good VHF through L band amplifier designs incorporate some resistive loading to limit gain and improve stability.

Passive Component Modeling

Passive components such as chip capacitors and inductors can exhibit unusual high frequency characteristics due to package parasitics. As a first order approximation, a chip capacitor has some associated lead inductance which can be modeled as a single inductor in series with the capacitor. This is shown schematically in Figure 12.

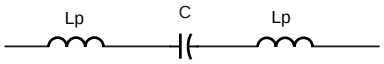

Figure 12. Capacitor Modeled with Lead Inductance

Tests conducted on a sample of high quality microwave chip capacitors suggest a combined lead inductance between 0.7 and 0.8 nH for capacitors in the 1 to 27 pF range. A high quality 1000 pF capacitor had 1.2 nH of associated lead inductance.

A wirewound chip inductor can also have a small amount of shunt capacitance distributed across the turns of the coil. Figure 13 shows schematically the parasitic capacitance in parallel with the inductor.

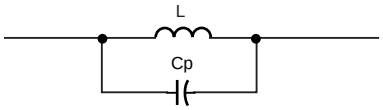

Figure 13. Inductor Modeled with Shunt Capacitance

Tests indicate the equivalent shunt capacitance can vary from 0.05 to 0.17 pF for chip inductors in the 4 to 27 nH range. If the series resistance, E.S.R., is known it can also be added into the model for each device. Circuit simulation accuracy will be improved immensely if the component parasitics are included in the simulation. Most component manufacturers have developed models for their products which they make available.

Sample Computer Simulation

An accurate circuit simulation can certainly provide the appropriate first step to a successful amplifier design. Manufacturing tolerances in both the active and passive components often prohibit perfect correlation. Besides providing important information regarding gain, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

The HBFP-0405 is analyzed in a 900 MHz circuit with the use of Libra for Windows. The input and output matching networks were optimized for best return loss. This simulation was the basis for the HBFP-0405 amplifier design presented in this application note. The actual circuit was optimized on the bench for best input return loss with greater emphasis placed on noise figure and IP3 as compared to output return loss. None the less, the simulation gives the designer a good starting point, especially in the area of broadband stability analysis. The circuit simulation is shown in Appendix A.

The parasitics associated with the chip capacitors and inductors were included in the simulation. The chip resistors were assumed to be ideal. In reality, there is some shunt capacitance which could influence the effect of R3 on the resonant frequency of the circuit consisting of L3 and C6. At low frequencies where R1 and R4 offer a resistive termination to the Q1, the capacitance across these resistors is probably insignificant.

At 900 MHz, the discontinuities associated with bends and corners of the microstriplines are not as significant as they would be at higher frequencies. As a result they are sometimes not simulated as their electrical length at 900 MHz may be small. A situation that may still necessitate careful modeling of microstriplines is in the area of the base terminal of the transistor. It is generally desirable that the circuit has as near unconditional stability as possible from VHF to as high a frequency that the device has gain. It is possible that the etch between the base of the transistor and L1 and the L1 mounting pad could provide the reactance that could cause high frequency instabilities with the transistor. At higher frequencies, such as in the 6 to 10 GHz frequency range, the reactance of L1 is fairly high, being only limited by the parasitic capacitance across L1. The parasitic capacitance could resonate with the circuit attached to the base. Most importantly, remember that proper circuit simulation could prevent undesired oscillations from occurring once the circuit is built up. The importance of accurate simulation of the emitter grounding has already been addressed.

The simulated noise figure, gain, and input and output return loss of the HBFP-0405 amplifier is shown in Figures 14, 15, and 16. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss and stability. A plot of Rollett Stability factor K is shown on Figure 17. As long as the emitter inductance is not increased appreciably, the main contributor to lack of stability will be in-band gain. Resistor R3 is used to enhance in-band stability.

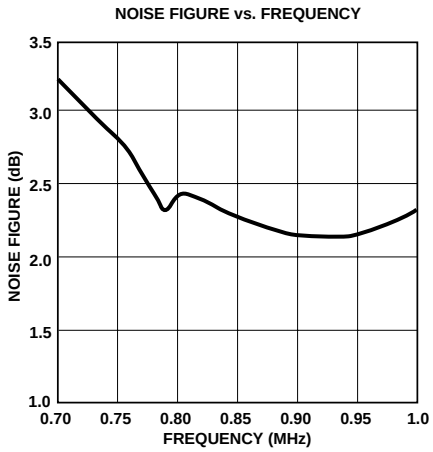

Figure 14. Noise Figure vs. Frequency

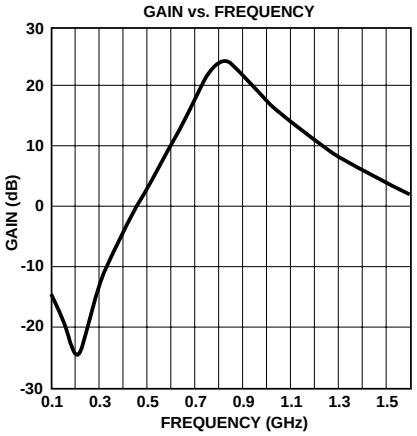

Figure 15. Gain vs. Frequency

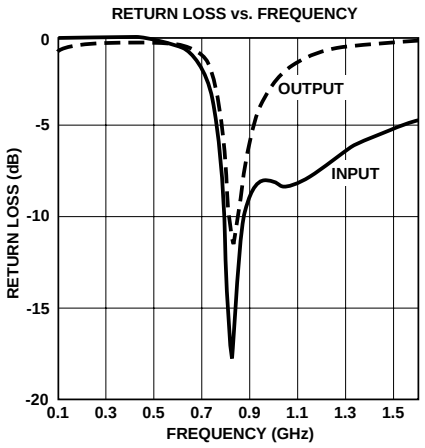

Figure 16. Input and Output Return Loss vs. Frequency

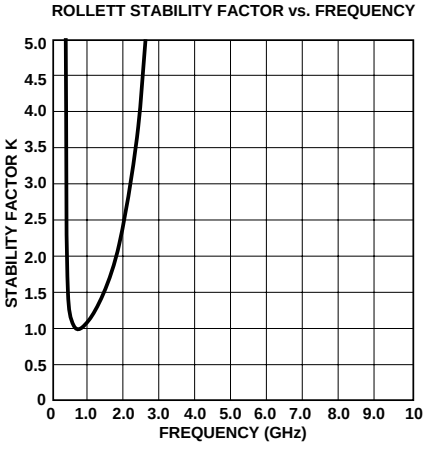

Figure 17. Rollett Stability Factor vs. Frequency

Appendix A

```
!HBPF-0405 800 MHz LOW NOISE AMPLIFIER
!SINGLE STAGE AMPLIFIER DESIGN
!SIMULATION BASED ON USING GENERIC DEMO TEST BOARD
!PARASITICS FOR PASSIVE COMPONENTS ARE INCLUDED
!BIAS CONDITIONS Vce = 2V, I = 5 mA
!SHUNT RESISTANCE IN COLLECTOR CIRCUIT FOR STABILITY
!A.J.WARD 8-18-98

DIM
    FREQ GHZ
    IND  NH
    CAP  PF
    LNG  IN

VAR

    LL1=.04  !EMITTER LEAD LENGTH, NEED TO DOUBLE IN LAYOUT FOR USING
    TWO EMITTER LEADS


CKT
    MSUB    ER=4.8   H=.031   T=.0014      RHO=1          RGH=0
    TAND    TAND=.01
    !INPUT MATCHING NETWORK
    MLIN    1        2        W=.05        L=.1
    SLC     2        3        L=.8         C=2.2          !C1
    MLIN    3        4        W=.05        L=.06
    MCROS   4        5        6            7  W1=.05  W2=.05  W3=.05  W4=.08
    SLC     5         8       L=.25        C=.8           !C7
    VIA     8        0        D1=.03  D2=.03  H=.031  T=.0014
    MLIN    6        9        W=.05  L=.06
    MSTEP   9        10       W1=.05  W2=.1
    MLIN    10       11       W=.1  L=.05
    IND     11       12       L=18                        !L1
    CAP     11       12       C=.08        !CAPACITANCE ACROSS COIL
    SLC     12       18       L=.25  C=1.3                !C8
    VIA     18       0        D1=.03  D2=.03  H=.031  T=.0014
    MLIN    12       13       W=.1  L=.05
    MSTEP   13       14       W1=.1  W2=.02
    MLIN    14       15       W=.02  L=.03
    MSTEP   15       16       W1=.02  W2=.012
    MLIN    16       17       W=.012  L=.001
    IND     7        20        L=430                      !L2
    CAP     7        20       C=.15  !CAPACITANCE ACROSS COIL
    MTEE    20       21       22  W1=.1  W2=.1  W3=.1
    SLC     22       23       L=1 C=47                    !C2
    VIA     23       0        D1=.03  D2=.03  H=.031  T=.0014
```

```
        RES     21      25      R=50                    !R1
        MLIN    25      26      W=.1  L=.1
        SLC     26      27      L=1.2  C=1000           !C3
        VIA     27      0       D1=.03  D2=.03  H=.031  T=.0014

        S2PA    17      50      40  C:\S_DATA\BJT\hbfp405b.s2p
        MLIN    40      0       W=.05   L^LL1
        !S AND NOISE PARAMETER FILES ALREADY INCLUDE VIAS,
        !LL1 REPRESENTS ADDITIONAL LEAD LENGTH/INDUCTANCE
        !ADDED IN SERIES WITH DEVICE EMITTER LEADS, LL1
        !SHOULD BE DOUBLED AND USED IN BOTH EMITTER LEADS
        !THEREFORE IF LL1 = .040 INCHES, THEN .080 INCHES
        ! OF MLIN IS ADDED TO EACH EMITTER LEAD.

        MLIN    50      51      W=.012  L=.001
        MSTEP   51      53      W1=.012  W2=.02
        MLIN    53      54      W=.02  L=.02
        MSTEP   54      55      W1=.02  W2=.05
        MLIN    55      56      W=.05  L=.05
        MLIN    56      57      W=.05  L=.2
        SLC     57      59      L=.75  C=1.7            !C6
        MLIN    59      61      W=.05  L=.25
        IND     56      62      L=10                    !L3
        CAP     56      62      C=.13   !CAPACITANCE ACROSS COIL
        RES     56      62      R=360                   !R3
        MTEE    62      63      64  W1=.15  W2=.15  W3=.1
        SLC     64      65      L=.8  C=47              !C5
        VIA     65      0       D1=.03  D2=.03  H=.031  T=.001
        RES     63      66      R=50                    !R4
        SLC     66      67      L=1.2  C=1000           !C4
        VIA     67      0       D1=.03  D2=.03  H=.031  T=.0014
        DEF2P 1   61 AMP

FREQ
        SWEEP   2       10      .1
        !STEP   0.8
        SWEEP   .1      2       .01

OUT
        AMP     DB[S11]
        AMP     DB[S21]  GR1
        !AMP    DB[S12]
        AMP     DB[S22]
        AMP     NF
        AMP     K       GR2
        !AMP    B1
        !AMP    NPAR
        !AMP    GA
```

```
!GRID
        !FREQ   .1      2       .1
        !GR1    1       20      1
        !GR2    0.5     1.5     0.5
OPT
        FREQ    0.8     .8
        AMP     DB[S21]>19
        AMP     DB[S11]<-13
        AMP     DB[S22]<-13
        AMP     NF<2
        AMP     K>1
```

www.hp.com/go/rf
For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or (408) 654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data Subject to Change

5968-2386E (12/98)