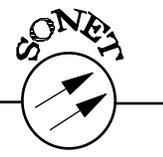
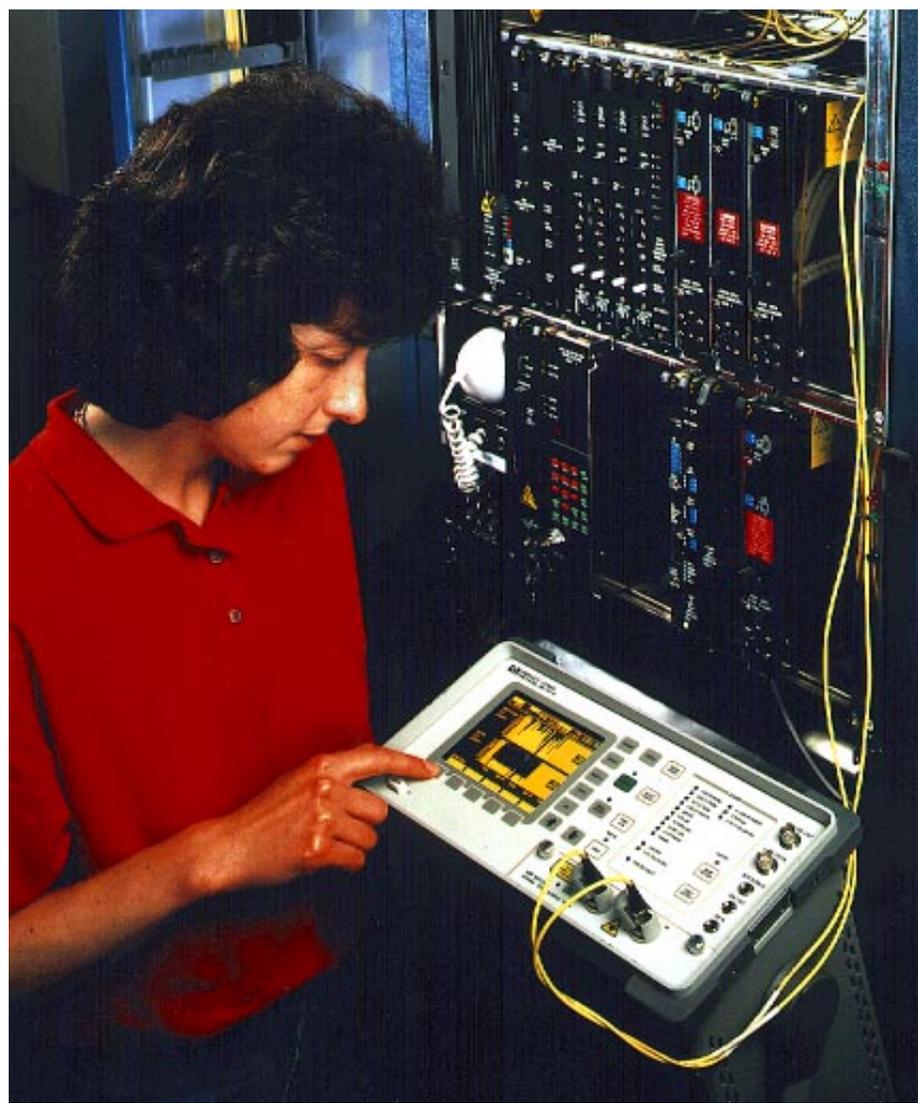

Evaluating Tributary Jitter from the SONET Network

Application Note 1252



Introduction

The innovation of using pointers to track the position of the Synchronous Payload Envelopes (SPE) within SONET signals has produced many benefits that will minimize the cost and complexity of network equipment. For example, SONET removes the need for back-to-back multiplexers/demultiplexers in cross-connects and add/drop multiplexers by enabling any customer payload to be located and tracked without the need to dismantle the multiple layers of hierarchy within the structure. However, due to the large inherent phase step associated with a pointer movement (i.e. 8UI per pointer movement), compared to that produced by pulse stuffing techniques used in asynchronous multiplexing, the SONET network has the potential of creating large jitter transients in the demultiplexed tributary outputs. The need to characterize the jitter performance of demultiplexers is being considered by Standards Committees such as T1X1.3., at the time of writing (1993).

The network architecture

In the long term, the synchronous SONET network may develop to the state where asynchronous networks will only exist at the periphery of the synchronous network, and all transport through the network is on SONET. However, this is an ideal model that may not be prevalent until well into the next century. At present, and during this intervening period as the SONET network evolves, the hybrid synchronous/asynchronous network will predominate. Thus a signal may experience several synchronous/asynchronous conversions during its passage through the network.

As SONET equipment is installed in the network, SONET islands will appear. Initially, these SONET islands are likely to be point-to-point networks. As the SONET portions of the network increase, these islands will merge to form larger more sophisticated islands consisting of not only Path Terminating Equipment (PTE) but also Add/Drop Multiplexers (ADM), Digital Cross-connect Systems (DCS), etc. As the tributary signal traverses these larger SONET islands as part of an SPE, phase and/or frequency differences between SONET network elements will induce pointer activity in the SONET signal. The impact of this pointer activity will be to increase the jitter on the asynchronous tributary signal passing out of the SONET island. This will produce

an accumulation of jitter on the tributary signal as it traverses the multiple islands in its transmission path.

For the long term network development scenario, (when end-to-end SONET transmission is prevalent), the jitter performance of the terminating PTE will be the main contributor to jitter on the demultiplexed tributary signal. However, until reaching this stage of development, the network will become filled with SONET islands. A tributary signal's transmission path may involve traversing multiple SONET islands, and the problem of jitter accumulation will exist.

Analysis of the network

In order to specify the jitter limits on a PTE, analysis has been performed to predict the expected jitter accumulation that might occur as a tributary signal passes through multiple SONET islands [1]. As a result of this analysis, a transmission path model has been produced which consists of 32 SONET islands, each containing 10 pointer processing Network Elements [2], (Figure 1).

To ensure that the jitter accumulation does not cause service degradation at the output of the last SONET island, the total network jitter must not exceed that specified for the tributary rate [3]. Therefore, each PTE must not only meet this specification but will have to exhibit a far better performance if the jitter at the output of the 32nd SONET island is to meet this requirement.

With the size and structure of the network model agreed, work is underway to allocate the amount of jitter which can be generated by the various jitter producing effects to ensure that the total network jitter does not exceed the specified limit on a tributary signal. As an example, the DS3 Interface Specification requires that the peak-to-peak jitter shall not exceed 5UI, (in the 10Hz to 400 kHz range). In order to achieve this with the 32 island model, the present proposal is to limit the maximum jitter from a PTE to 1.3UI. Table 1 shows how this budget has been allocated between mapping jitter, single pointer movements and degraded synchronization conditions.

Characterization of jitter performance

Test sequences were developed by T1X1.6 during the 1988-90 timeframe and have since been incorporated into the Bellcore standard, TR-NWT-00253 [4]. These sequences aimed to emulate expected network degradations.

During 1992, Telecom Canada carried out testing to verify the theoretically predicted responses to various types of pointer activity on PTEs [5]. As well as verifying the theoretically predicted responses to variations in pulse stuffing ratios (used to map the tributary signal into the SPE), and to single pointer movements, Telecom Canada also showed that the defined tests did not fully represent the pointer sequences that a real network might produce.

With the results from the practical experimentation and the recent specification of jitter performance in terms of three network conditions, (an example of which is shown in Table 1), T1X1.3 have reviewed the pointer movement sequences. The aim is to produce tests that more closely emulate real network conditions and also allow measurement of the specified jitter thresholds. Also, as a further result of the experimentation, it has become clear that Test Methodology guidelines need to be produced in order to achieve accurate and repeatable results.

Figure 1 Hybrid network model

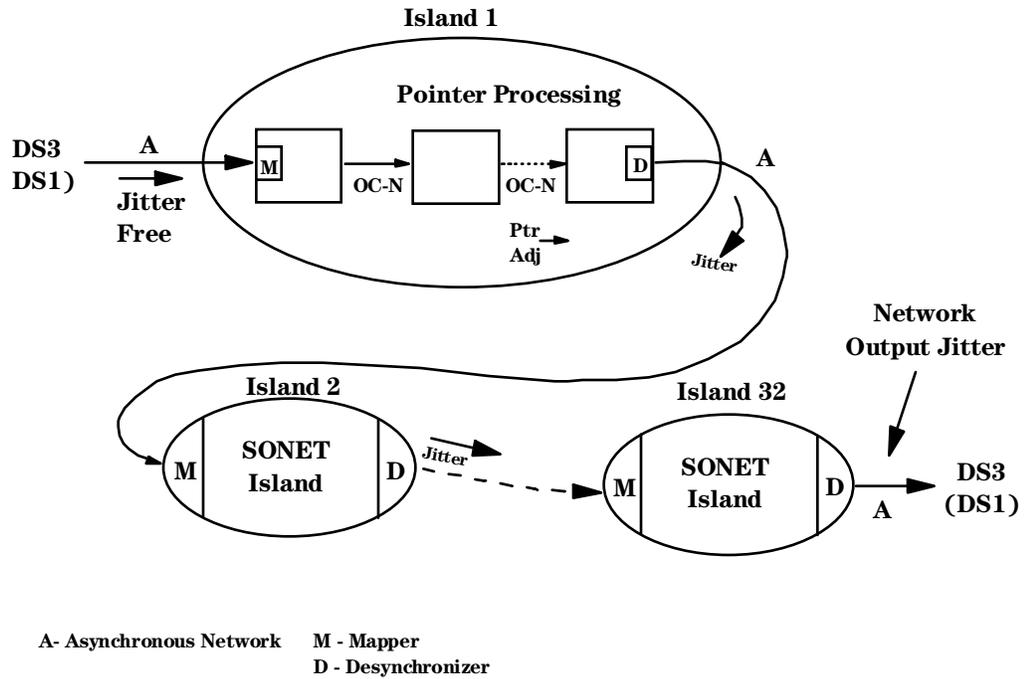


Table 1 Jitter specification for a DS3 signal demultiplexed from a single SONET island

Jitter category	Jitter allocation (Ulp-p)	
	A0	A0 + 0.30
Mapping jitter (Note 1)	A0	0.40
Single Isolated Pointer	A1	A0 + 0.30
Degraded Synchronization Conditions	A2	1.3

Notes

1. Jitter from a SONET island in which there is no pointer activity.
2. The DS3 will be jitter free as it enters the SONET island.
3. These values are under study.

Figure 2(a) Single Isolated Pointer test

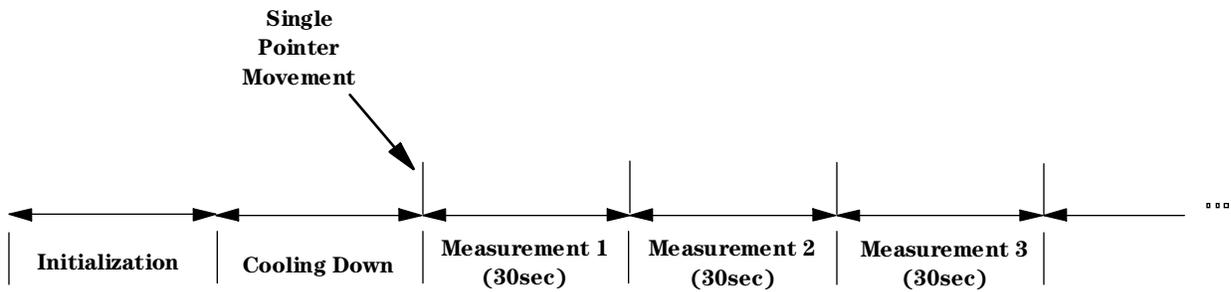
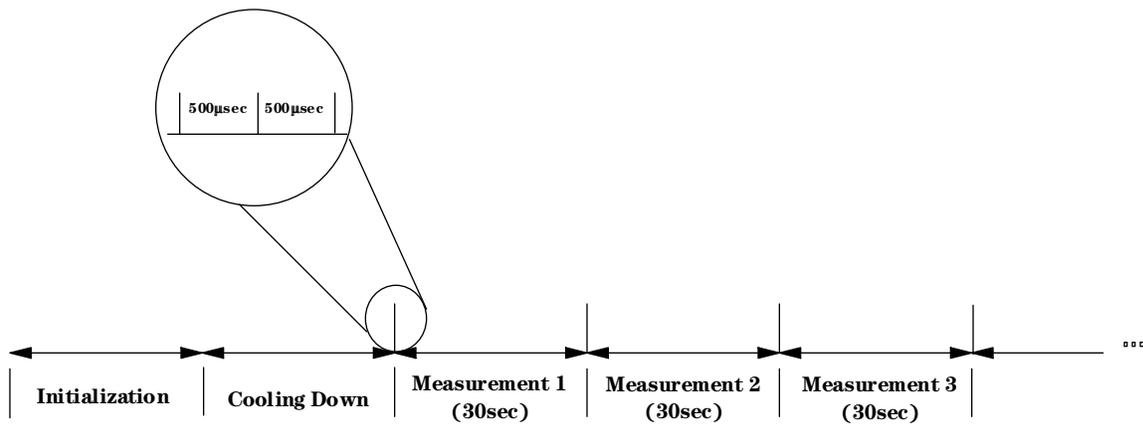


Figure 2(b) Burst-of-3 test



The new test sequences

The first criterion to be met is when there is no pointer activity. This test requires the frequency of the tributary signal to be varied to find the maximum jitter produced due to the pulse stuffing ratio used to map the tributary signal into the SPE i.e. **Mapping Jitter**. This test checks the specification of the maximum jitter on the output due to the process of extracting the tributary signal from the SPE.

The second criterion defines the response to a **Single Isolated Pointer** movement. This is tested using a sequence which has a single pointer-movement every 30 seconds, Figure 2(a).

The pointer movements are spaced 30 seconds apart in order to allow time for the effects of each movement to completely die out before another pointer movement is applied. This ensures that the resultant jitter measured is that produced by a single pointer movement.

Two test sequence have been defined to measure the performance of a PTE in a **Degraded Synchronization Condition**. The first test emulates the network condition where phase noise in a chain of network elements (e.g. ADMs, cross-connects, etc) accumulates to produce a burst of pointers with minimum spacing. Figure 2(b) shows the test defined to cover this condition.

Like the single pointer test, the bursts are set 30 seconds apart to allow time for the effects of each burst to die out before the next burst is applied.

The second test emulates the network condition when the originating PTE loses lock to the system clock. This condition will cause continuous pointer movements to be generated. On top of this background, extra pointer activity may occur due to phase noise from the other nodes of a network. Therefore, on top of the background of continuous pointer movements, an added or canceled perturbation to the background sequence is performed every 30 seconds.

In the original sequences, the clock synchronization loss was represented by continuous evenly spaced pointer movements. However, this is not always the case in practice. Experimentation has shown that gaps are generated in the pointer sequence due to the effects of the positioning of the SONET Overhead bytes. For example, when an STS-SPE is cross-connected, a repetitive sequence of 87 evenly spaced pointer movements followed by a gap equivalent to 3 missing pointer movements is generated. Table 2 shows the effect on the jitter output from the 87/3 sequence compared to that produced by the original Periodic Test Sequence.

Similar effects can be predicted for all types of SONET SPEs. It is possible by the use of sophisticated pointer processing nodes to remove this effect and produce regular, evenly spaced pointer movements. However, this is not specified as a requirement for the network equipment, and as the most straightforward techniques produce this effect, PTEs will have to be designed to cope with this sequence.

Figure 2(c) shows the new sequence that has been defined to emulate the clock synchronization loss condition for DS3 testing.

Table 2
Experimental results showing effect of 87/3 sequence

Pointer sequence	Jitter on demultiplexed DS3 (UIp-p)
Periodic sequence from T1X1.6	0.15
87/3 sequence	0.60

Notes

- 1 In both cases, the pointer spacing was set at 33msec, equivalent to a frequency offset of 4.6ppm.
- 2 The results were obtained by testing the DS3 drop port from the HP 37704A SONET test set.

Figure 2(c) - Periodic pointer adjustment test sequence

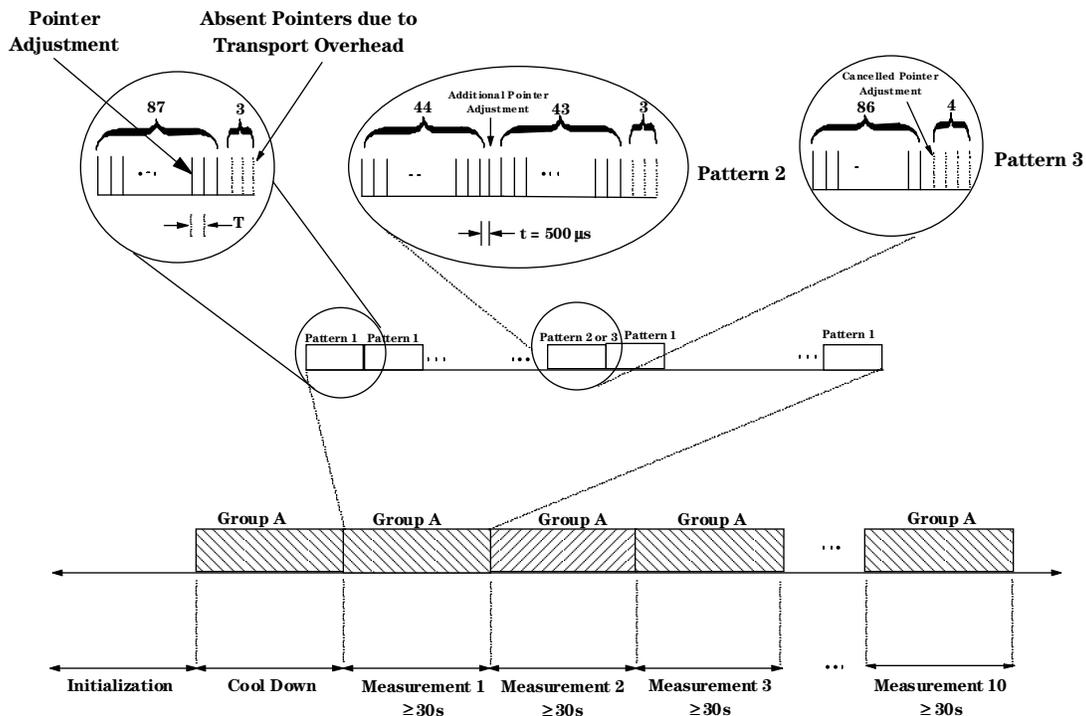


Figure 3 Typical block diagram of a DS3 PTE

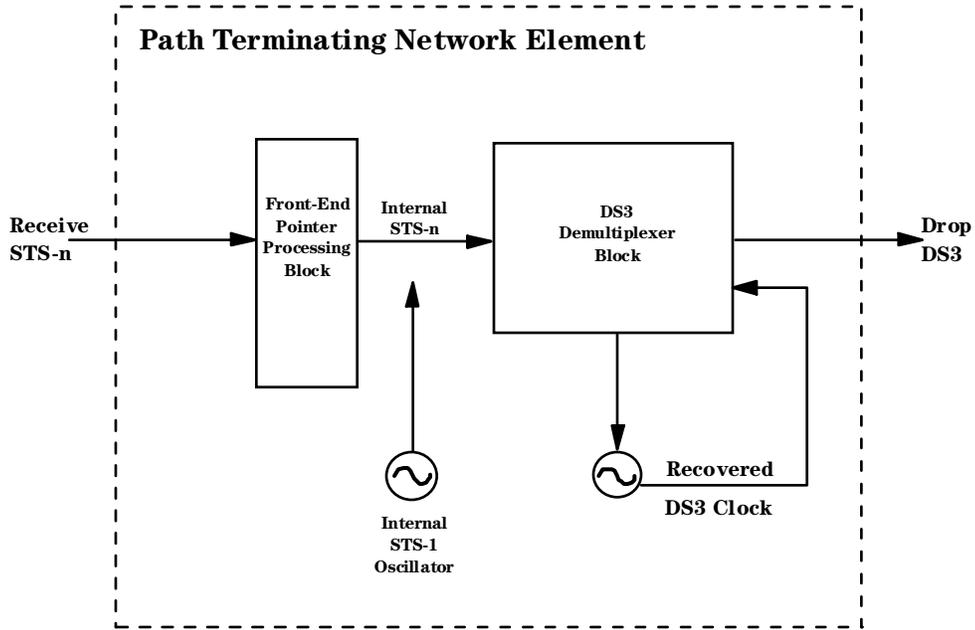
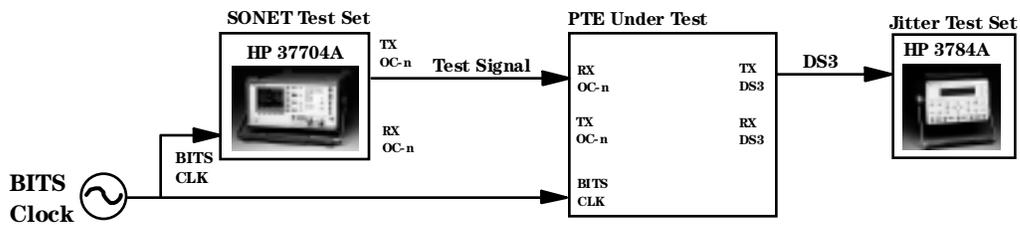
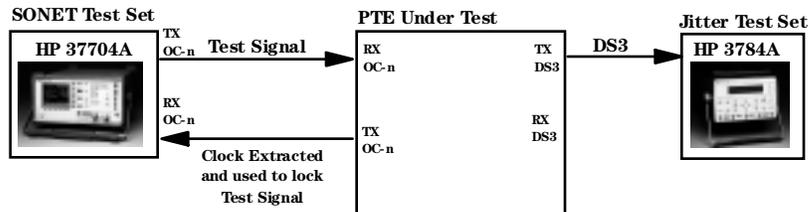


Figure 4 PTE test configuration



(a) Synchronize Test Set to PTE by frequency locking Test Set's Transmitter to the BITS Clock used by PTE.



(b) Synchronize Test Set to PTE by frequency locking Test Set's Transmitter to the Clock extracted from the SONET signal generated by the PTE.

Test methodology

As a side-effect of the practical experimentation being carried out, it became clear that there was a need to clarify the test methodology in order to obtain accurate and repeatable measurements. Factors like the number of repetitions of each pointer sequence test are being considered, to produce implementation guidelines for each test sequence. Two of the most important requirements arise from the structure of the PTEs available today.

By testing PTEs which demultiplex DS3, it has been found that many contain front-end pointer processing blocks that extract the SPE from the received signal and pass it into an internally generated STS-n before the signal is demultiplexed to extract the DS3 signal, Figure 3.

For effective testing of a PTE with this architecture, it is imperative that the frequency of the internal STS-n signal is locked to the frequency of the test signal being applied to the PTE. If this is not accomplished, frequency and/or phase differences between the two STS-n signals will produce pointer activity on the internal STS-n signal. These pointer movements will produce spurious spikes of jitter on the output DS3. Figure 4 shows two possible test configurations which will synchronize the test signal to the PTE and hence avoid this problem.

The second effect of this structure comes from the elastic store which will be present in the front-end pointer processing block. This store will absorb some of the pointer activity in the received STS-n signal before producing any pointer movements in the internal STS-n signal. (Cases have been observed where as many as 15 movements are absorbed.) If a pointer sequence test is performed, it is necessary to prime this elastic store to ensure the pointer sequence applied to the PTE is that which appears at the input to the Demultiplexer Block. (This can be achieved by applying a test signal containing continuous pointer movements of the same polarity as those used during the testing until jitter spikes are detected on the tributary output each time a pointer movement occurs in the test signal).

Summary

By tightly specifying the jitter generated by PTEs before there is significant deployment of SONET equipment, network operators can avoid major problems once the 32 island scenario becomes a reality. The definition of sequences which simulate real network conditions, accompanied by Test Methodology guidelines, will allow network operators to gain confidence that equipment they are installing in their networks will interwork with the existing asynchronous networks both now and in the future.

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1. B. Powell, "Multiple SONET Islands Jitter Simulation Results", Alcatel, T1X1.3/91-092R1, November 1991
2. T1X1.2, "SONET Hypothetical Reference Circuit (HRC)", T1X1.2/93-015, March 1993.
3. ANSI, "Digital Hierarchy Electrical Interfaces", T1.102-199X, November 1991.
4. Bellcore, "Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria", TR-NWT-000253, Issue 2, December 1991
5. K. Mahon, "Significance of Telecom Canada's SONET Jitter Accumulation Measurements", Telecom Canada, T1X1.3/92-129, November 1992.

Appendix

Network emulation model for a SONET test set

Introduction

The fundamental objective of any test set transmitter is to reproduce, in a controllable and repeatable fashion, signals which are true representations of conditions in a real network. To produce a SONET Test Set which meets these criteria when generating OC-n signals containing pointer movements, the concept of a Network Emulation model aids in highlighting the important characteristics of such a signal.

A SONET network

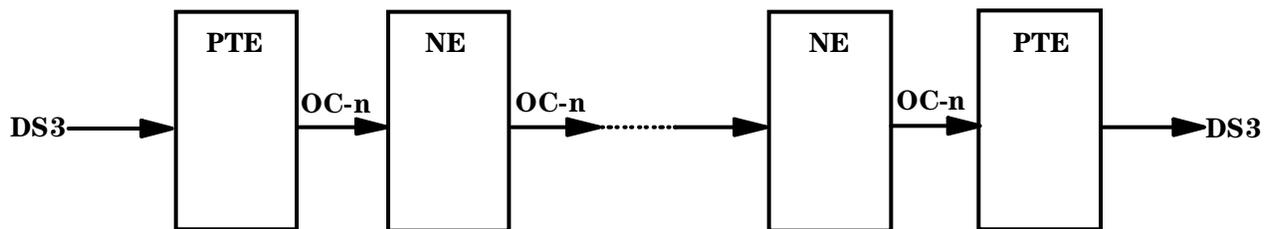
Figure A1 shows a typical SONET transmission network. The tributary signal, which in this example is a DS3, enters the network through Path Terminating Equipment (PTE). This element maps the DS3 into an SPE in the OC-n signal. At the far end, the terminating unit demultiplexes the OC-n signal and reconstitutes the DS3 tributary signal. Along the SONET transmission path, the OC-n may pass through various SONET Network Elements which are pointer processing nodes e.g. digital cross-connects.

At the entry point to the network, the frequency variations from nominal DS3 Rate are catered for by pulse stuffing the DS3 as it is mapped into the SPE.

There will be no pointer movements in the OC-n signal out of the first element, only variations in pulse stuffing rate, (which handles all frequency and phase variations). Pointer movements are induced in the transmission path when an SPE is transferred between OC-n signals i.e. as it passes through a Network Element which is a pointer processing node.

It is important to notice that when a pointer movement is induced in the network, there is no effect on the pulse stuffing ratio used to map the DS3 into the SPE, (as this is always defined at the entry point to the SONET network). Therefore, the pulse stuffing ratio will remain constant during any pointer activity, with this ratio being defined by the long term average SPE rate relative to the DS3 rate.

Figure A1 Typical SONET transmission network



Test set emulation model

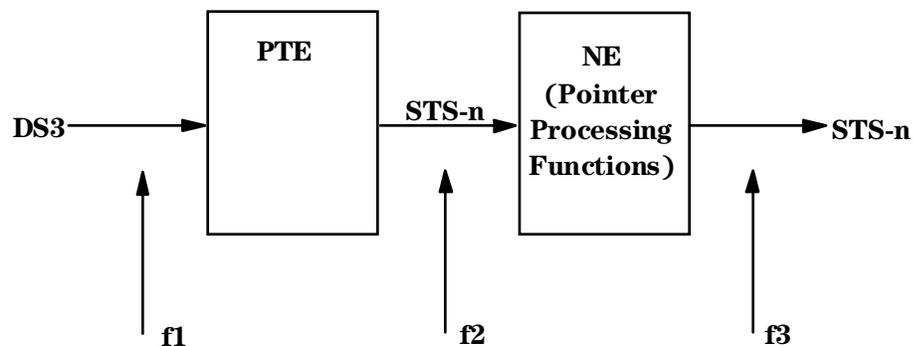
The reduced network model which must be emulated in order to accurately reproduce signals containing pointer movements, consists of a PTE plus a network element which provides pointer processing functions. Figure A2 shows the emulation model. In this model, the pulse stuffing rate is controlled by the relative frequency of the DS3 Rate (f_1) to the internal STS-n Line Rate (f_2). The rate of pointer additions is controlled by the relative frequency of the internal STS-n line rate (f_2) to the output STS-n line rate (f_3). With this model, (as in the real network), when pointer movements are introduced, there will not be a step change in the pulse stuffing rate around the pointer movement to counteract the apparent step change in SPE Rate.

The defined Pointer Test Sequences consist of repetitive patterns of pointer movements, all of which are the same polarity. This implies that an offset exists between the line rate (f_3) and SPE rate (controlled by f_2). As the definition for the sequences requires that the line rate remains constant, the internal STS-n (f_2) rate must change to generate these pointer movements. Changing f_2 will also cause a step change in the pulse stuffing ratio. A step change of this nature would not occur in the network as line frequencies are restricted by network equipment specifications from suddenly changing rate. The initialization period defined at the start of the sequences provides time for the effects of the step change to die out before the jitter measurements are performed.

Summary

By defining a test set transmitter in terms of a Network Emulation Model, it is possible to highlight, and hence ensure reproduction of the important characteristics of signals containing Pointer Movements. This model clarifies the need for the pulse stuffing process to be independent from the generation of pointer movements. The implementation of this emulation model in a SONET Test Set will ensure accurate production of the stimuli required to measure the tributary jitter performance of a terminating PTE.

Figure A2 Test set emulation model



Pulse Stuffing Rate controlled by $f_1 \leftrightarrow f_2$

Pointer Movement Rate Controlled by $f_2 \leftrightarrow f_3$



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