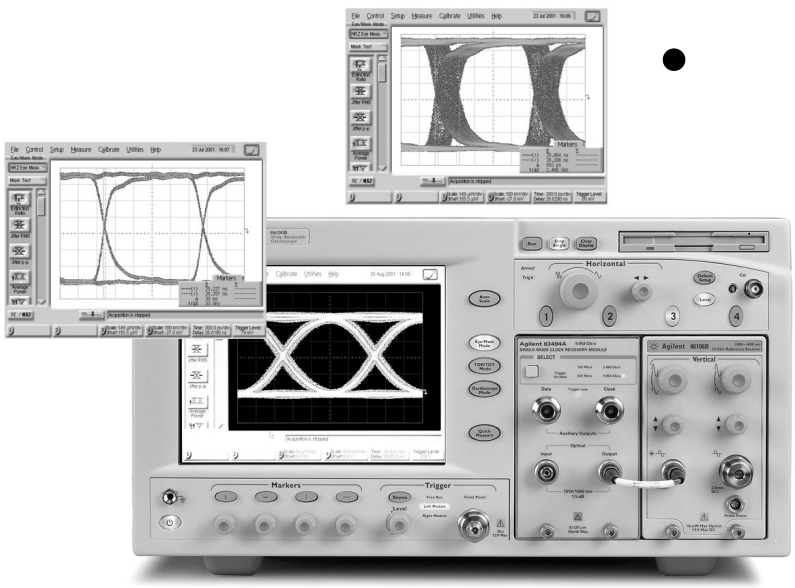
Loop Bandwidth and Clock Data Recovery (CDR) in Oscilloscope Measurements

Application Note 1304-6



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Abstract

Time domain measurements are only as accurate as the trigger signal used to acquire them. Often times, an external trigger signal is unavailable, so the trigger must be derived from the data stream itself. However, this process itself has an effect on the measurement. Because the incoming signal has a certain amount of jitter, or phase noise, the clock recovery system should be able to account for it. On the other hand, it is often necessary to measure the amount of jitter on the signal and very wide bandwidth clock recovery systems mask this jitter. The 8349xA clock recovery modules for the 86100B Infiniium digital communications analyzer offer two separate bandwidth settings, allowing the user to choose a very clean signal, or a very accurate jitter representation.

Introduction

Almost all sampling oscilloscope measurements require some type of external trigger signal. A real time oscilloscope takes several samples in quick succession after each trigger pulse, as shown in Figure 1. Very high-speed signals cannot be accurately measured on a real time oscilloscope. Equivalent time oscilloscopes typically have less internal jitter and noise as well as much higher bandwidth, so are better suited for making jitter measurements. As illustrated in Figure 2, an equivalent time sampling oscilloscope acquires each data point after a different trigger pulse. As a result, accurate measurements are only possible if the trigger signal remains accurately aligned to the data. If this alignment is not achieved, the individual data points will not be placed accurately in time. When an external trigger is unavailable, the trigger signal must be derived from the data itself. This process is known as Clock and Data Recovery (CDR). Unfortunately, this process greatly effects the measurement. Just how it affects the signal is dependent on the properties of the CDR circuit. Because every signal has a certain amount of jitter or phase noise, it is vital that the CDR circuit can compensate for that jitter. At the same time, it is important to be able to measure that jitter, so the CDR circuit must not mask it. The most important part of a CDR circuit is a Phase-Locked Loop (PLL).

The properties of the PLL will have the greatest effect on the over all CDR performance. Unfortunately, this is a trade off, the wider the loop bandwidth (also called noise bandwidth or single-sided loop bandwidth) of the PLL, the better it will track the signal, but the more it will mask the actual jitter on the signal. A narrow loop bandwidth will have more trouble tracking the signal, but will result in a cleaner clock signal and will give a more accurate representation of the true signal.

This trade off is very similar to the trade off which is made in receiver circuits. Receivers in digital communications systems almost always require some type of phase synchronization circuit that accurately determines the start and end of the bit period. This is vital for the decision circuit to make symbol determinations at the correct time.

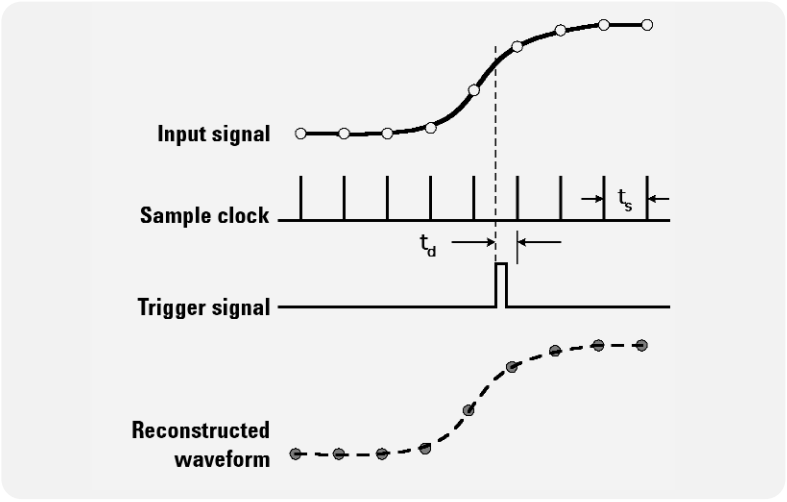

Figure 1. A real-time scope acquires several data points after each trigger pulse.

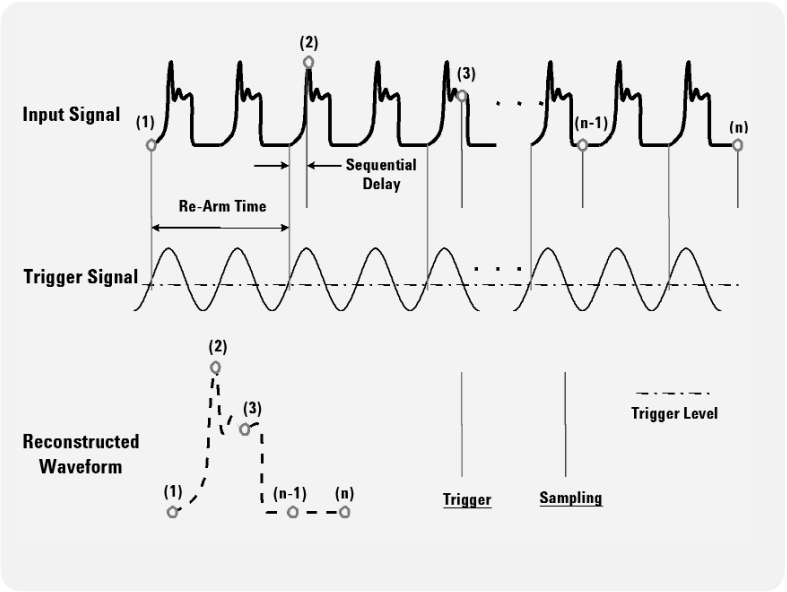

Figure 2. An equivalent time oscilloscope acquires each datum after a different trigger pulse.

If the loop bandwidth is very narrow, the system will have trouble acquiring and maintaining an accurate phase lock. However, the wider the loop bandwidth, the more the input signals phase noise will be transferred through the circuit.

Phase-Locked Loops and Clock Data Recovery

A traditional phase-locked loop is a feedback that consists of three parts: a phase detector, a loop filter, and a voltage controlled oscillator (VCO). A phase detector is a device with two inputs and an output that is proportional to the phase difference between the two inputs. The first input is the PLL input and the second is the output of the VCO. This can be as simple as an analog mixer but most modern circuits use some kind of digital circuit. A loop filter is typically a low pass filter that takes the output of the phase detector and attenuates the high frequency components. For example, an ideal analog mixer will have two frequency components, one at the sum of the frequencies of the inputs and one at their difference. If the frequencies are very near each other, which is the case in locked PLL, the second term will be essentially a DC term proportional to the sine of the phase difference. At small phase differences, the sine of the phase difference is very close to the phase difference. If the phase detector has a positive or negative output, dependent on the input leading or lagging the derived clock signal, the LPF can be replaced by an integrator circuit. In the case of a digital phase detector, the output is often a pulse train where the frequency of the pulses is proportional to the phase difference. The loop filter can be a simple low pass filter or a digital counter. The VCO is an adjustable oscillator that will change output frequency depending on its input voltage. By shifting frequency, the phase difference between the input and the VCO is closed. A simple schematic of a PLL is shown in Figure 3.

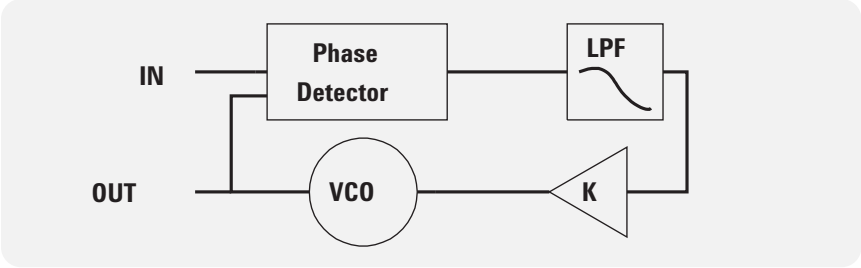

Figure 3. A simple PLL schematic.

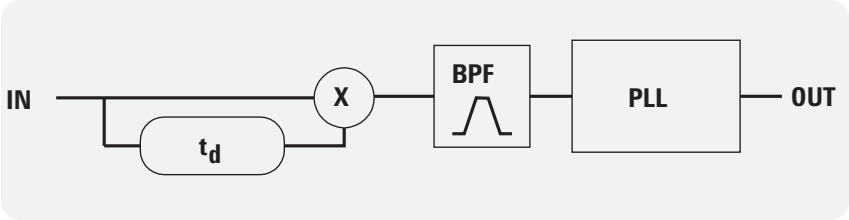

Figure 4. A simple CDR circuit using a hard delay, a band-pass filter, and a PLL.

$$S(\omega) = \left[\sum_{m=-\infty}^{\infty} \delta\left(\omega - \frac{m\omega_b}{L} \right) \right] \frac{L+1}{L^2} \sin c \left(\frac{\omega}{\omega_b} \right)^2 - \frac{1}{L}\delta(\omega)$$

Equation 1. The frequency spectrum of a 2N-1 PRBS. L is the length of the pattern in bits and is the bit frequency.

In order to recover the clock data from a data stream, some components have to be added to the front end of the PLL in order to isolate a frequency component at the data rate. An added complication is that in many commonly used patterns, such as a non-return to zero, pseudo-random bit sequence (NRZ PRBS), there is a frequency null at the data rate and every one of its harmonics (see Equation 1). This means that a simple band-pass filter cannot be used to isolate data rate frequency component. Although there are several ways to create this component, probably the easiest conceptually is to split the signal, delay one branch by one half bit period, and then mix the two parts back together. This will create pulses with a duration of one half bit period, and therefore a frequency component at the data rate. If that mixed signal is then fed into a narrow band-pass filter around the data rate, the result is a sine wave at the data rate. The output of the filter is then fed into the PLL. A diagram of this circuit is shown in Figure 4.

It is also possible to modify the phase detector of the PLL such that the data input is fed directly into the phase detector and no additional circuitry is required before the PLL. In such a circuit the phase detector is really tracking the clock transitions versus the transitions in the data rather than performing a true phase comparison.

Loop Bandwidth, Jitter, and Phase Noise

Ideally, the input signal to a PLL is a perfect sine wave and the output will pull in and match that output perfectly. However, in any real word signal there is going to be noise in frequency, amplitude, and phase. The PLL has to be able to maintain a lock in the presence of noise but it must not be so sensitive that a very small signal change will cause noise on the output. The abilities of a CDR circuit to deal with noisy signals will be primarily determined by the characteristics of its PLL. One of the most important characteristics of a PLL is its loop bandwidth. The loop bandwidth is defined as the integrated magnitude of the PLL frequency transfer function over the entire frequency spectrum. It is essentially a measure of how well the PLL performs in the presence of noise. The signal to noise ratio (SNR) of the PLL output is equal to the SNR of the input times the ratio of the input noise bandwidth to the loop bandwidth times two (Equation 2). The phase noise of the PLL output is equal to the phase noise of the input times the ratio of the loop bandwidth to the input noise bandwidth times pi (Equation 3). A very narrow loop bandwidth will reject most noise and will give a very clean output, however, it will have trouble maintaining a phase lock on a noisy signal as the time between lock losses can be shown to be proportional to the SNR of the output. The exact opposite is true of a wide bandwidth PLL: it will track noisy signals very well, but the output will itself be somewhat noisy. So there is an obvious trade off between noise sensitivity and the loops ability to track the signal. In a communications system, a very narrow bandwidth PLL will be used where the signal is fairly clean or where very accurate triggering is paramount. A wider bandwidth PLL is needed for applications where the signal becomes noisy or where it is not so vital for the clock data to be absolutely accurate.

$$(SNR)_o = \frac{(SNR)_i B_i}{2B_L}$$

Equation 2. The output SNR (SNRo) is dependent on the input SNR (SNRi), the input noise bandwidth (Bi), and the loop bandwidth (BL)

$$\overline{\Theta}_{n2}^2 = \overline{\Theta}_{n1}^2 \frac{2B_L}{B_i}$$

Equation 3. The output phase noise is dependent on the input phase noise, the loop bandwidth(Bi), and the input noise bandwidth (BL)

In a measurement application, the same sort of tradeoff has to be made. One has to remember that the displayed data is really the time of the signal versus the trigger signal, not some absolute time base. The measured jitter is really the jitter of the signal versus the trigger signal. A very narrow loop bandwidth CDR circuit will give a very accurate depiction of the jitter on the signal as the triggering will have very little noise. However, if you are trying to measure a very noisy signal, a narrow bandwidth CDR will often lose it's lock, or may not be able to achieve it in the first place. A wider bandwidth CDR will do a better job of tracking the signal as the recovered clock data will very accurately match each individual bit. Unfortunately, this masks some of the jitter on the data. The recovered clock accurately tracks the data and its jitter. As a result, the recovered clock and the data are very closely related, therefore, using the measured jitter to be much less than the actual jitter on the signal. On the other hand, the narrow bandwidth CDR's recovered clock would stay more true to the true signal clock so the jitter would be more accurately represented. Figures 5 and 6 show the same signal using a narrow and a wide loop bandwidth.

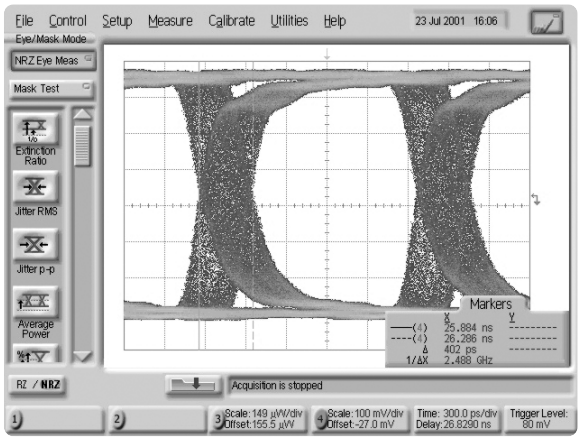

Figure 5. A narrow loop bandwidth results in a more accurate representation of the jitter.

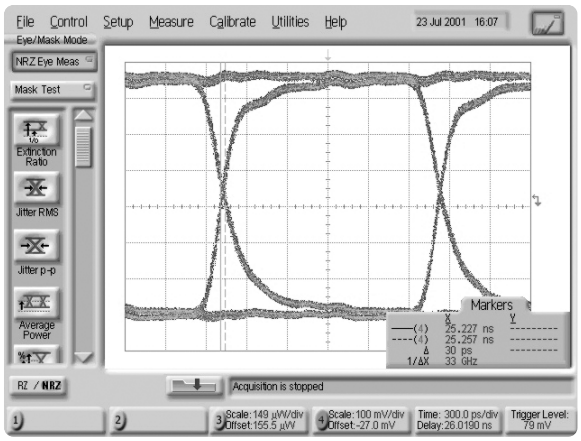

Figure 6. A wide loop bandwidth results in a very clean measurement of the signal.

Conclusion

When measuring a signal, it is very important to get a very accurate representation of that signal. A very narrow CDR is ideal for this application. On the other hand, sometimes excessive jitter will mask important features, or to recover clock data at all, so it is also important to be able to filter out much of the jitter. This can be accomplished with a wide bandwidth CDR. A CDR system with flexible loop bandwidth offers the advantage of covering both applications.

Appendix A: References

Best, Ronald, *Phase-Locked Loops; Design, Simulation, and Applications*, McGraw-Hill Professional Engineering, San Francisco, 1999.

Blanchard, Alain, *Phase-Locked Loops; Application to Coherent Receiver Design*, Wiley-Interscience, New York, 1976.

Klapper, Jacob, *Phase-Locked and Frequency-Feedback Systems*, Academic Press, New York, 1972.

Sklar, Richard, *Digital Communications; Fundamentals and Applications*, Prentice Hall, New Jersey, 1988.

Appendix B: A Simple Simulation

The effects of loop bandwidth can be easily simulated in a program such as the Agilent Advances Design System (ADS). One such circuit can be seen in figure B-1. For the sake of simplicity, both of the circuit and mathematically, a simple passive lead-lag filter is used. A lead-lag filter consists of two resistors and a capacitor. The components are connected in series and the output voltage is measured across the second resistor and the capacitor. This circuit is ideal as an example it can be shown that the loop bandwidth is approximately equal to one forth of the corner frequency of the loop filter, as long as the capacitance is small compared to the reciprocal of the loop gain. This can be calculated as the reciprocal of the sum of the resistances multiplied by the capacitance (Equation B.1, derivation in Appendix C). This means that by simply adjusting the loop filter parameters, the loop bandwidth can be adjusted and the simulation can measure the resultant total phase noise. The simulation shows that for very narrow loop bandwidths, the phase noise on the output is very small. This means that the recovered clock would be very pure and as such would result in a very accurate measurement of the signal. If the loop bandwidth is very large, the noise on the output tracks the total noise on the system. In such a case, the measurement would track the input signal very well and would filter out most of the input's phase noise.

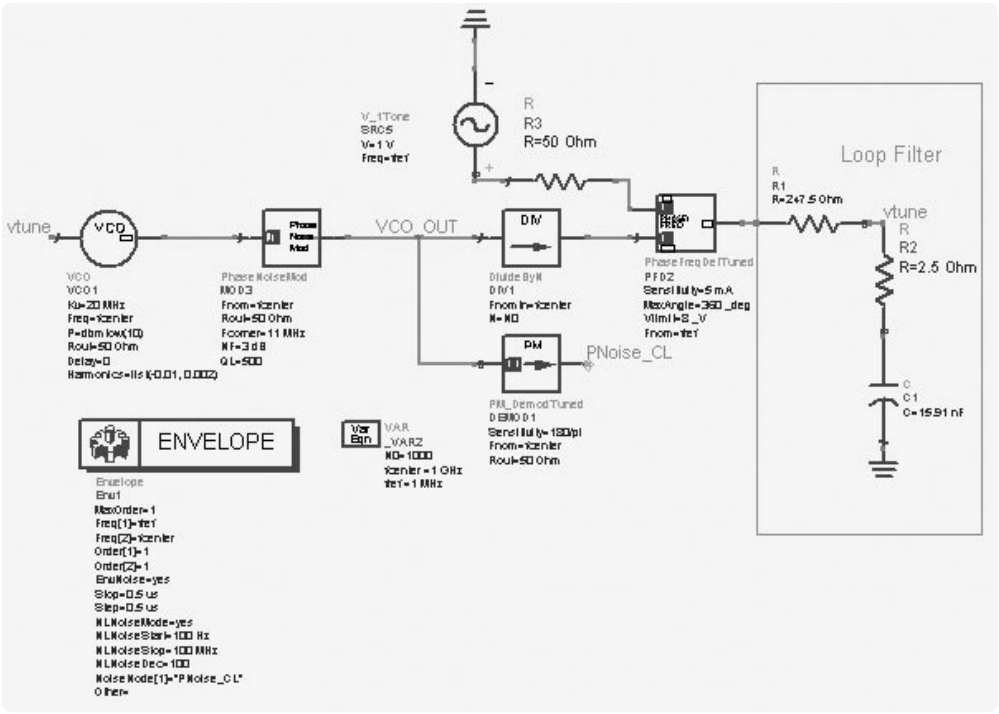

Figure B. 1 - A simple PLL model in Agilent ADS with a passive lead-lag loop filter.

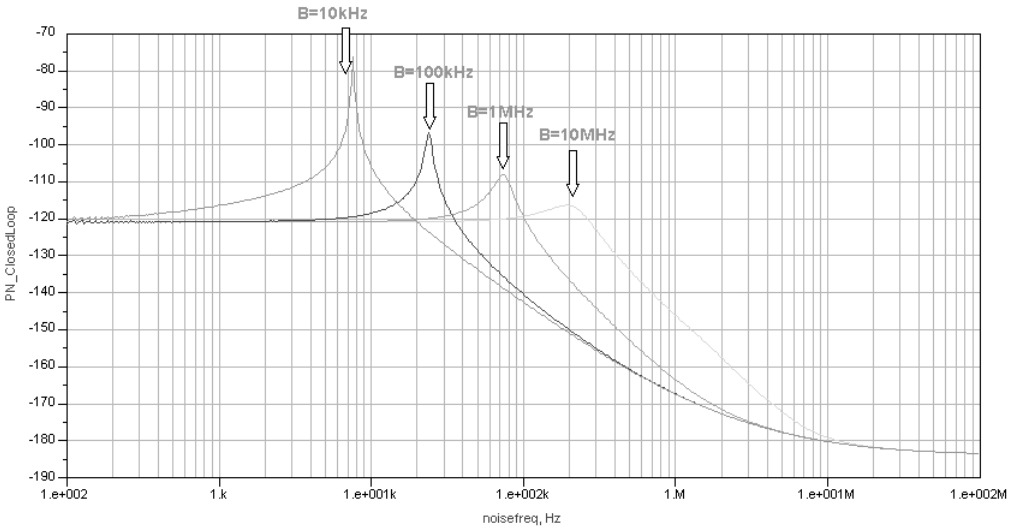

Figure B. 2 - The output phase noise of the PLL in Figure A.1 is related to the loop bandwidth of the filter. The different shapes of the curves are due to the change in damping factor with the change in filter parameters.

$$B_l \approx \frac{1}{4C(R_1 + R_2)} \quad KC << 1$$

Equation B.1. The loop bandwidth of this PLL is very closely related to the filter parameters.

Appendix C - Mathematical Derivations

The phase transfer function of a PLL as shown in figure 1 with a passive lead-lag filter is shown in Equation C.1 through C.3.

$$H(s) = \frac{K\dfrac{1+s\tau_2}{\tau_1+\tau_2}}{s^2 + s\dfrac{1+K\tau_2}{\tau_1+\tau_2} + \dfrac{K}{\tau_1+\tau_2}} = \frac{(1+s\tau_2)\omega_n^2}{s^2+2s\omega_n\zeta+\omega_n^2}$$

Equation C. 1

$$\omega_n = \sqrt{\frac{K}{\tau_1+\tau_2}}$$

Equation C. 2

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K}\right)$$

Equation C. 3

$$\tau_1 = R_1C \quad \tau_2 = R_2C$$

Equation C. 4

The loop bandwidth can then be calculated as in equation C.5

$$B_L = \int_0^\infty \left|H(j\omega)\right|^2 d\omega = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

Equation C. 5

By combining equations C.2 through C.5, we get equation C.6

$$B_L = \frac{1}{4}\left(\frac{C^2R_2^2K + C(3R_2+R_1) + \dfrac{1}{K}}{C^2(R_1R_2+R_2^2) + C\dfrac{R_1+R_2}{K}}\right)$$

Equation C. 6

In almost all cases, C will be much less than 1/K, so we can ignore all but the left most terms in both the numerator and the denominator. After canceling 1/K, equation C.7 is obtained. This shows that the loop bandwidth can be very easily and closely estimated from the filter parameters.

$$B_l \approx \frac{1}{4C(R_1+R_2)} \qquad C << \frac{1}{K}$$

Equation C. 7

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5988-6682EN

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