Debugging Parallel RapidIO Designs with the Agilent 16700 Series Logic Analysis System

Application Note 1436

Who should read this application note?

This document is for designers of digital systems incorporating parallel 8-bit RapidIO interconnections such as internet routers, DSL access multiplexers, wireless base stations, and defense and medical imaging applications. It describes the procedure for debugging systems incorporating RapidIO parallel interconnects using the Agilent 16700 Series logic analysis system. The designer is guided through the process of probing the RapidIO links, analyzing signal integrity using the eye scan capability of the 16760A logic analyzer, and performing bus analysis and protocol decode using the N4215A software tool set for RapidIO.

The Agilent products in this application note include an E5387A soft touch, connectorless probe, a low-load, differential 17-channel adapter for the 16760A logic analysis module. The 16760A offers interchangeable probing front ends to support a wide range of debug and validation applications for embedded microprocessor and microcomputer-based designs. The N4215A software tool set provides text-based decoding of data captured by the 16760A module and a special-purpose trigger library, which enables RapidIO protocol triggering and real-time filtering of Idle control symbols.

These tools also work for 16-bit parallel RapidIO implementations at speeds of up to 1.5 Gb/s (750 MHz clock double data rate or DDR). This application note describes only the setup for parallel, not serial, 8-bit implementations running at speeds of up to 800 Mb/s (400 MHz DDR). Note the distinction between bit times (shown as Mb/s or Gb/s) and clock rates (shown as MHz). For most of this document, speeds will be referred to in bit times, not in clock rate. The bit times are also “per channel”, not an effective total throughput.

For information regarding probing design guidelines for speeds up to 1.5 Gb/s, please contact your Agilent representative, who will put you in touch with an application engineer.

RapidIO overview

RapidIO is a chip-to-chip interconnect standard that was developed by a consortium of companies known as the RapidIO Trade Association. The interconnect is designed for high-speed I/O with low latency for use in control operations in the communications industry—such as internet routers, DSL access multiplexers, and wireless base stations—and defense and medical imaging applications. Many other high-speed interconnects are designed for optimal data transmission speed, but these are less useful in control applications because large data transmissions prevent quick responses to short control messages. RapidIO is a point-to-point, packet-switched connection, unlike past control buses such as PCI. For this reason, system topologies must incorporate some kind of switching fabric to accommodate linking to multiple devices.

Figure 1 shows an example system design incorporating RapidIO links in an internet protocol (IP) router. A single system controller communicates to packet forwarding cards and a packet switch fabric subsystem through a RapidIO switch.

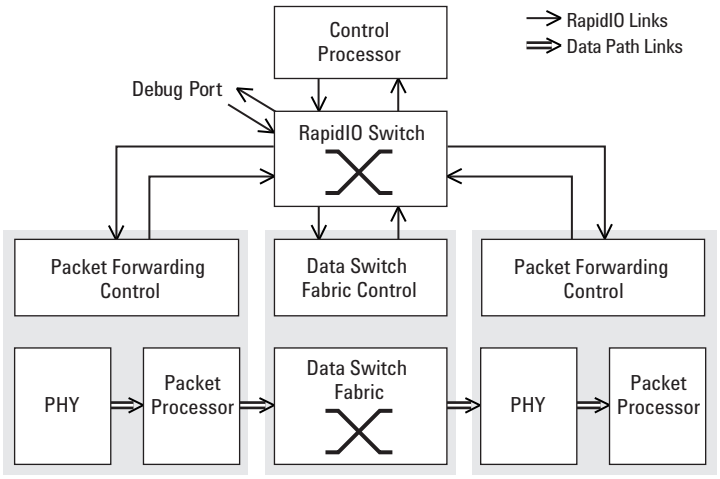


Figure 1. Example IP router design with RapidIO interconnects

Using E5387A soft touch connectorless probing

The Agilent E5387A soft touch connectorless differential probe combines second-generation probing technology with the lowest intrusion logic analysis probe currently in the market place. This technology produces tremendous improvement in probe-to-printed circuit board (PCB) connection reliability, a 4x reduction in required area for a probing connection, and true differential flow-through signal routing. All of these attributes produce a probe that is perfectly matched to the needs of high-speed interconnect measurement.

To better understand the soft touch probing technology, see Figure 2. Two rows of compliant spring pins connect with pads laid down on the surface of the PCB. These contacts provide an extremely low probe load (< 0.70 pF per channel), and make a good electrical connection with a small amount of compression force on a variety of standard PCB platings. Additionally, the pin contact points are free from the contamination effects that plague other connectorless probing technologies.

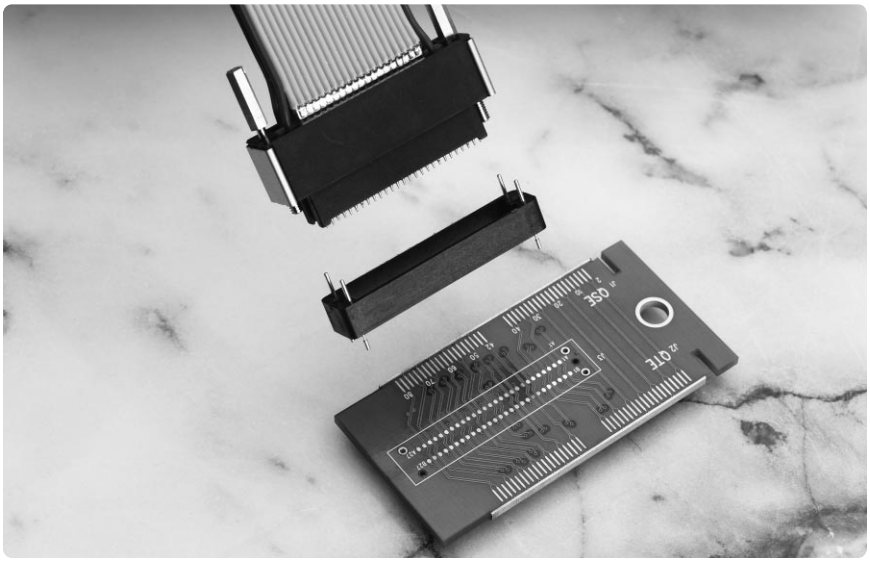


Figure 2. Connectorless E5387A probe and retention module for RapidIO

The probe is attached to the PCB via a retention module (middle of Figure 2), which ensures pin-to-pad alignment and provides the screw holes to hold the probe in place. The retention module makes NO electrical connection to circuit traces and is not to be confused with a connector. The E5387A probe includes five retention modules. Additional retention modules can be ordered separately.

On the E5387A probe footprint, the + and – connections for each signal are arranged across from each other (+ signals in one row, and – signals directly across in the other row). It is very easy to route differential signals with either pair polarity orientation while maintaining constant differential spacing. The pinouts shown in Table 1 are designed with RapidIO in mind; the clock signal is in the center of the data bus, not on the outer edge.

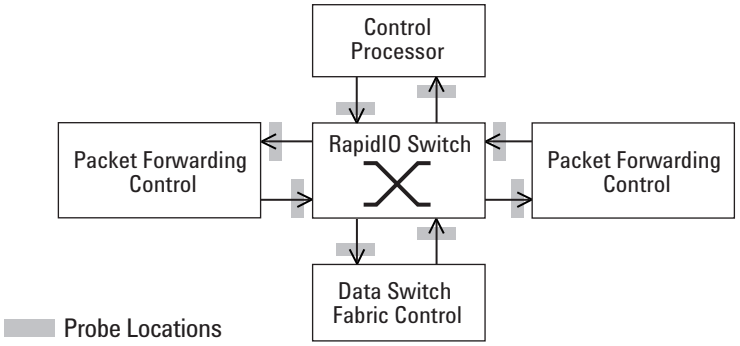


Figure 3. Probe connection locations

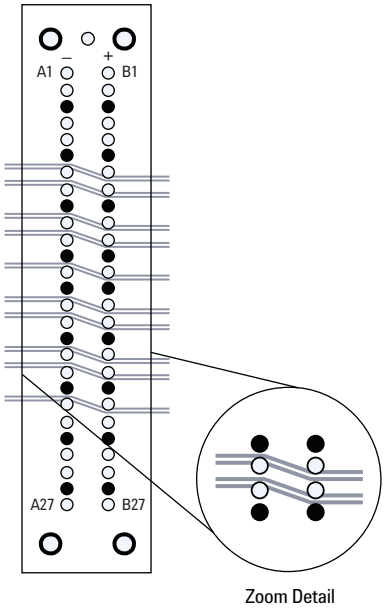


Figure 4. Recommended RapidIO board routing for probe connection

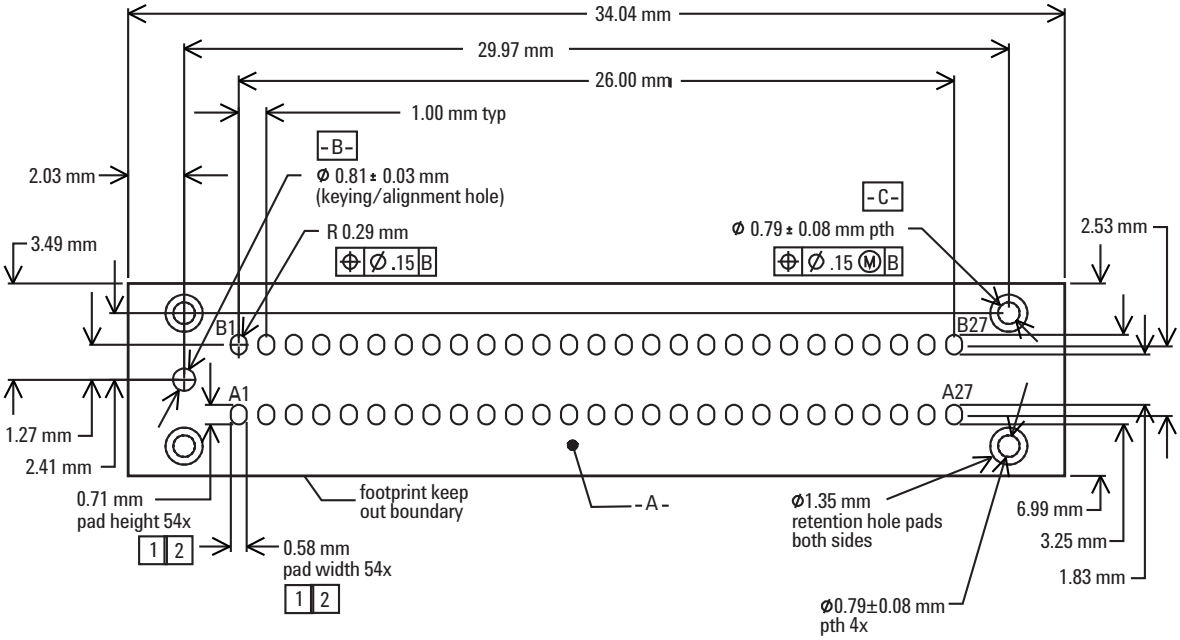
Therefore it is extremely simple to route a RapidIO bus through this footprint when using devices that comply with the RapidIO Interconnect Specification (see http://www.RapidIO.org for more information).

Due to the switched connections between subsystems, there is no longer a single probing point from which all control traffic can be seen. There are two debug strategies possible for such a system: an extra port on the RapidIO switch can be dedicated to debug purposes, or probe connections can be made on all of the possible links. The former is easier to implement, but the latter makes it possible to see multiple traffic streams simultaneously.

Using an extra switch port as a debug port, traffic between any source and destination device can be routed to the probe. The advantage to this strategy is you minimize board space used by probing locations and have the option of seeing traffic from different devices. Another advantage is that problems associated with capacitive probe loading are eliminated because the logic analyzer acts as the receiver of the data, instead of as a passive probe placed between sender and receiver. The disadvantage is that you can only see traffic from one link at a time and only from one direction of that link; because the debug port is a bi-directional link, only one side of that port can send traffic to the logic analyzer.

By probing multiple locations around a switch fabric, you can analyze data flow throughout the system. Multiple acquisition cards can also capture data simultaneously from multiple probe locations for a time-correlated view of the whole system, rather than just one link.

The best place to locate probes is as close as physically possible to the receiving device's termination. This enables the effects of the circuit board transmission lines to be measured with eye scan, and also minimizes the level of signal reflections seen at the probe. Figure 3 indicates where to locate probe connections on the example system from Figure 1. When probing signals between a sender and receiver, you must consider the effect of the probe on the signal. Figure 6 shows the electrical load model for the E5387A probe.



Notes:

1. Must maintain a solder mask web between pads when traces are routed between the pads on the same layer. Soldermask may not encroach onto the pads within the pad dimension shown.
2. Via in pad not allowed on these pads. Via edges may be tangent to pad edges as long as a solder mask web between vias and pads is maintained.
3. Permissible surface finishes on pads are HASL, immersion silver, or gold over nickel.
4. Footprint is compatible with retention module, Agilent part # 16760-68702.
5. Retention module dimensions are 34.04 mm x 7.01 mm x 4.98 mm tall relative to the top surface of the PDB. Retention pins extend 4.32 mm beyond the bottom surface of the RM through the PCB.
6. Assume normal artwork tolerances for pad size dimensions.

Figure 5. Mechanical footprint for E5387A soft touch, connectorless probe

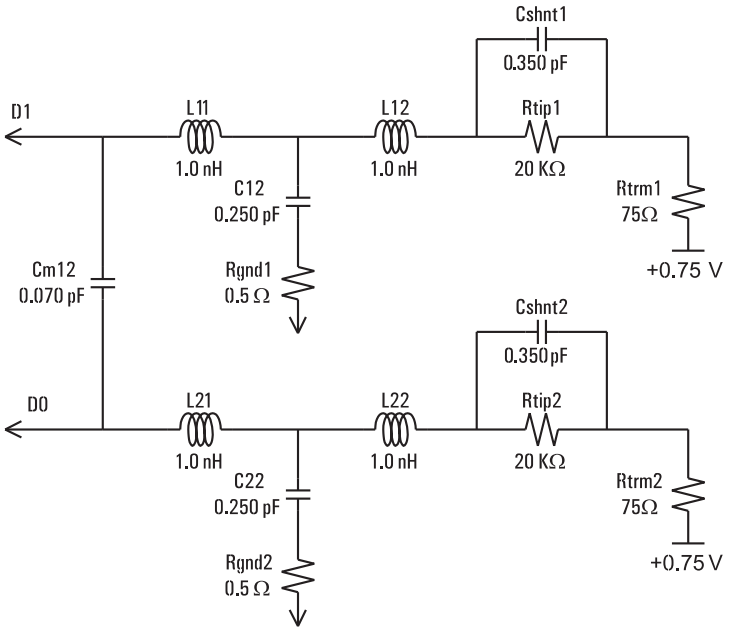


Figure 6. Electrical load model for E5387A probe

PAD#	Pod Input	RapidIO	PAD#	Pod Input	RapidIO
A1	nD0	(-) N/C	B1	D0	(+) N/C
A2	nD1 (-)	N/C	B2	D1 (+) N/C	
A3	**Ground**	N/C or GND	B3	**Ground**	N/C or GND
A4	nD2 (-)	N/C	B4	D2 (+)	N/C
A5	nD3 (-)	N/C	B5	D3 (+)	N/C
A6	**Ground**	Ground	B6	**Ground**	Ground
A7	nd4 (-)	TD0/RD0 (-)	B7	D4 (+)	TD0/RD0 (+)
A8	nD5 (-)	TD1/RD1 (-)	B8	D5 (+)	TD1/RD1 (+)
A9	**Ground**	Ground	B9	**Ground**	Ground
A10	nD6 (-)	TD2/RD2 (-)	B10	D6 (+)	TD2/RD2 (+)
A11	nD7 (-)	TD3/RD3 (-)	B11	D7 (+)	TD3/RD3 (+)
A12	**Ground**	Ground	B12	**Ground**	Ground
A13	nCLOCK (-)	nCLOCK (-)	B13	CLOCK (+)	CLOCK (+)
A14	**Ground**	Ground	B14	**Ground**	Ground
A15	nD8 (-)	TD4/RD4 (-)	B15	D8 (+)	TD4/RD4 (+)
A16	nD9 (-)	TD5/RD5 (-)	B16	D9 (+)	TD5/RD5 (+)
A17	**Ground**	Ground	B17	**Ground**	Ground
A18	nD10 (-)	TD6/RD6 (-)	B18	D10 (+)	TD6/RD6 (+)
A19	nD11 (-)	TD7/RD7 (-)	B19	D11 (+)	TD7/RD7 (+)
A20	**Ground**	Ground	B20	**Ground**	Ground
A21	nD12 (-)	FRAME (-)	B21	D12 (+)	FRAME (+)
A22	nD13 (-)	N/C	B22	D13 (+)	N/C
A23	**Ground**	Ground	B23	**Ground**	Ground
A24	nD14 (-)	N/C	B24	D14 (+)	N/C
A25	nD15 (-)	N/C	B25	D15 (+)	N/C
A26	**Ground**	N/C or GND	B26	**Ground**	N/C or GND
A27	N/C	N/C	B27	N/C	N/C

Table 1. Pinout table showing suggested 8-bit RapidIO connection to E5387A probe

```
.SUBCKT
ProbeLoadE5387A %"Sig0" %"Sig1"

#
#
# revA2: 20 Jul 2002
#
# BASED ON IN-CIRCUIT MEASUREMENTS MADE WITH
   AGILENT 8753E 6 GHz NETWORK
# ANALYZER AND AGILENT 54750A TDR/TDT USING 50 OHM TEST FIXTURE
#  accurately models probe load out to 6 GHz
#  including probe resonance
#  50 ohm trace-width = pad-width, routed through pad. SMT PADS NOT INCLUDED.
#
# 3-pin model with coupling between signal pairs. (see pinout)
# Signal pairs are lightly coupled for the following data pairs:
#  D0,D1 D2,D3 D4,D5 D6,D7 D8,D9 D10,D11 D12,D13 D14,D15
# Signal pairs are isolated from other signal pairs and clock by ground
#

Cm12 %Sig0 %Sig1 0.070pF

L11 %Sig1 %890 1.0nH
C12 %890 %919 0.250pF
Rgnd1 %919 %0 0.5
L12 %890 %904 1.0nH
Rtip1 %904 %903 20K
Cshnt1 %904 %903 0.35pF
Rtrm1 %903 %905 75
Vtrm1 %905 %0 DC 0.75V

Lpin21 %Sig0 %911 1.0nH
C22 %911 %920 0.250pF
Rgnd2 %920 %0 0.5
Lpin22 %911 %909 1.0nH
Rtip2 %909 %910 20K
Cshnt2 %909 %910 0.35pF
Rtrm2 %910 %912 75
Vtrm2 %912 %0 DC 0.75V

.ENDS ProbeLoadE5387A
```

Figure 7. Spice subcircuit model for testing probe loading

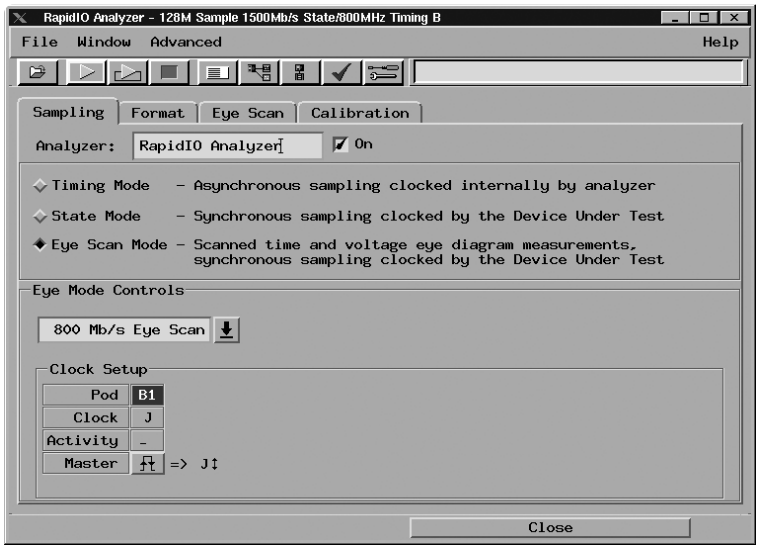


Figure 8. Sampling configuration of 16760A logic analyzer using both rising and falling clock edges

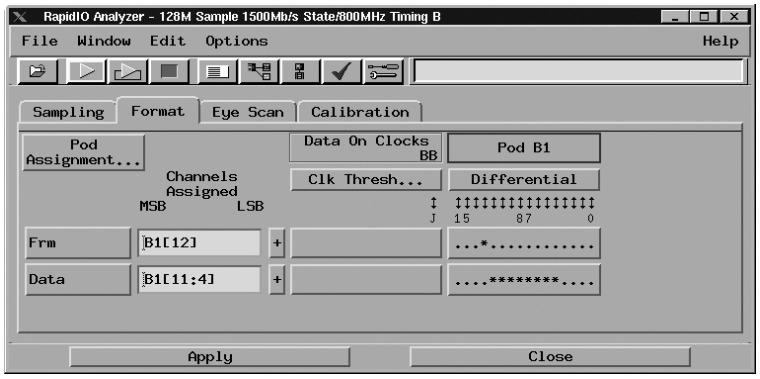


Figure 9. Format menu connecting bus signals to logic analysis pods and channels

Basic logic analyzer configuration

Once your probing connection is made, it's time to set up the logic analyzer. Because each RapidIO connection is comprised of two unidirectional links that operate with independent clocks, two separate 16760A logic analysis modules are required (if visibility in only one direction is sufficient, you can use a single module).

First, configure the sampling of the analyzer to use both rising and falling edges of the clock (see Figure 8). The double-edge clocking can be set in either State Mode (for synchronous data acquisition) or in Eye Scan Mode (for eye diagram measurements).

Next, configure the format of the logic analyzer (i.e., which bus signals connect to which pod and channel). If you follow the recommended pinouts from this document, your Format menu should look like Figure 9.

Note how RDAT[7:0] map to D1[11:4] (pod 1 of slot D), the middle 8 bits of the pod. Also note that this bus is labeled as the Receive link by prefacing the FRM and DAT labels with an R. The same settings apply to the Transmit link.

Examining signal integrity with eye scan

Eye scan is a recent advancement in logic analysis technology from Agilent. Using a 16760A module, input signals can be measured with 1 mV and 12 ps resolution to produce a comprehensive view of the entire interconnect. Eye scan technology is much faster than traditional scope-based signal integrity testing for validating that high-speed signals are correctly functioning. You no longer have to worry about wasting time debugging logical problems to find that the problem is a parametric or signal integrity one. Signal integrity regression testing of prototypes is now possible so that any change in system hardware or software can be quickly validated before logical testing.

To use eye scan with your RapidIO interconnect, first set your analyzer to eye scan mode in the “Sampling” tab of the setup window. Next, press the “Run” button, as shown in Figure 10.

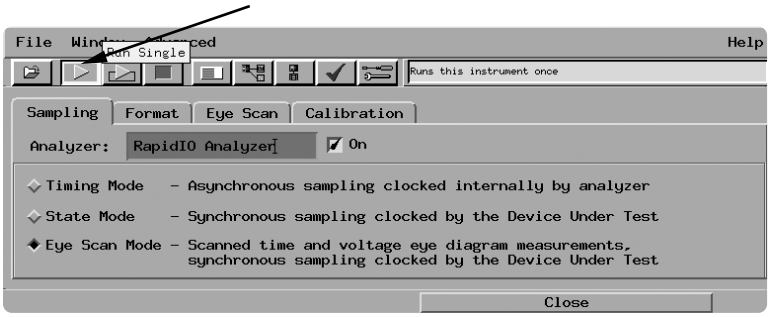


Figure 10. Setup for eye scan mode with arrow pointing to start button

You will begin collecting eye diagrams on all the signals of your RapidIO link simultaneously. The default settings run at fairly low resolution (50 ps steps in time by 50 mV steps in voltage) for a quick view.

Depending on the location of your probe, you may see reflections like the ones shown in Figure 11. The closer you place your soft touch probes to the receiving device, the better the picture. Consult the application note *Designing High-Speed Digital Systems for Logic Analyzer Probing,* publication number 5988-2989EN, at http://literature.agilent.com/litweb/pdf/5988-2989EN.pdf, for further information on optimizing your design for probing.

You can either view multiple overlays of data bus eyes or individual signals. For a high resolution view, the measurement resolution can be adjusted down to 10 ps and 10 mV steps. You can also choose to integrate each pixel for longer periods of time to capture very infrequent occurrences. Please see application note 1382-8 *Saving Time with Multiple-Channel Signal Integrity Measurements,* publication number 5988-5409EN, at http://cp.literature.agilent.com/litweb/pdf/5988-5409EN.pdf, for more information about eye scan.

Bus analysis and protocol decode

Using the N4215A software analysis tool set, you can decode RapidIO control symbols and packets as well as check for data integrity using the control symbol 16-bit complement and the packet CRC methods defined in the RapidIO specification.

First, as shown in Figure 12, configure the analyzer to run in "State Mode" (State Mode is synchronous sampling using the bus clock).

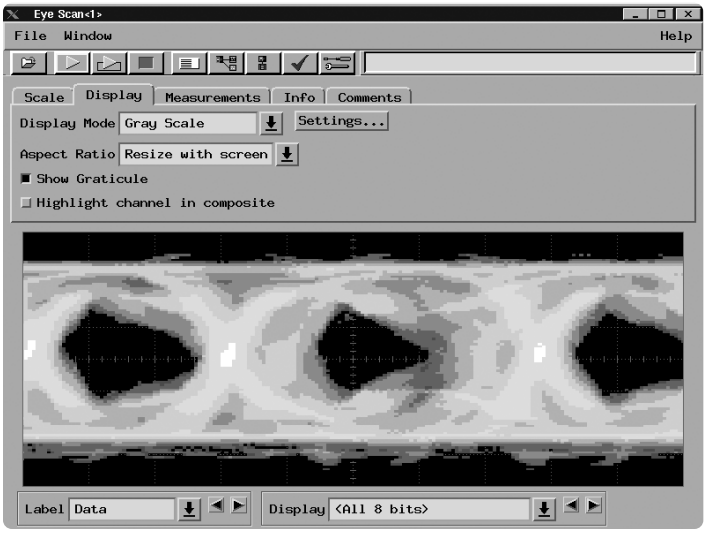


Figure 11. Eye diagrams collected on all signals simultaneously

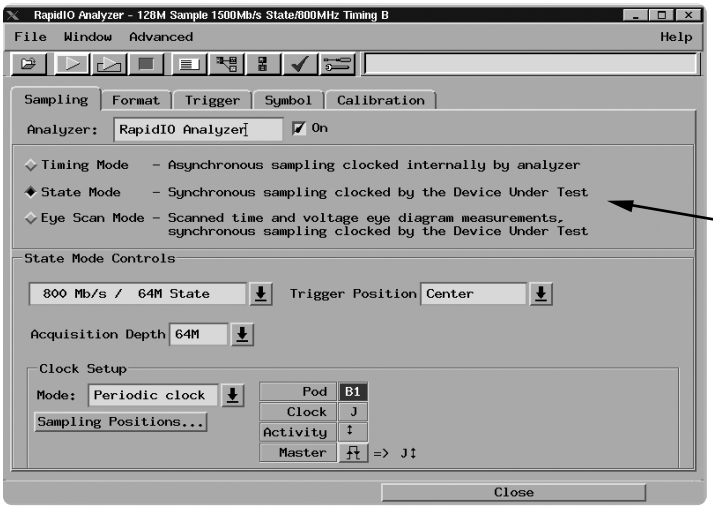


Figure 12. State mode configuration showing sampling on rising and falling clock edges

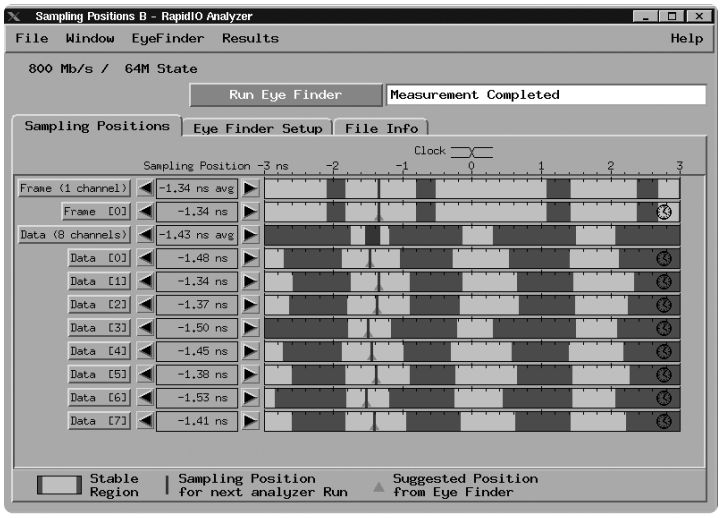


Figure 13. "Run Eye Finder" computes the data stable regions relative to the clock edges and automatically configures the sampling positions for each bus channel

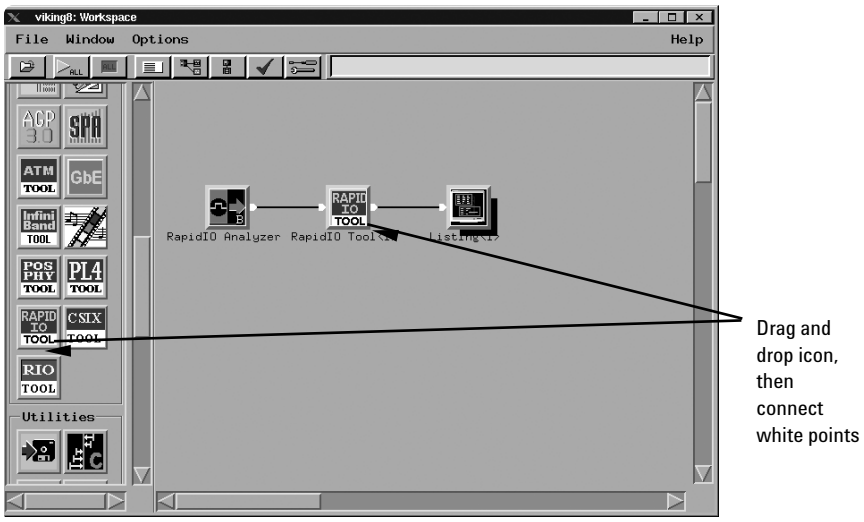


Figure 14. Setup for N4251A software analysis tool set for RapidIO

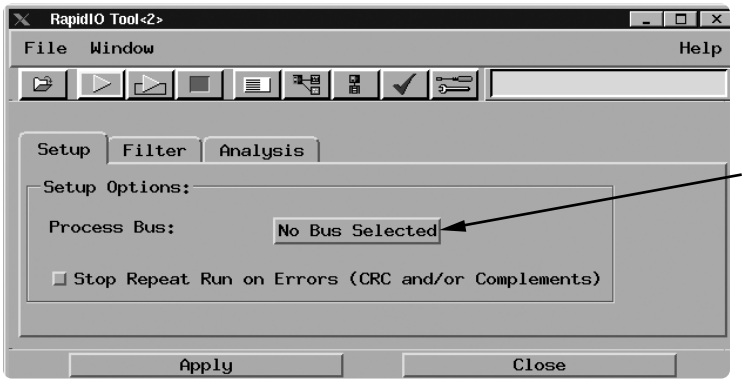


Figure 15. Configuration button for bus definition

Note the logic analyzer is sampling on both rising and falling edges of the clock. Now set the sampling positions relative to the clock edge. At high speeds, the analyzer's default settings probably aren't correct. Click on the "Sampling Positions" button and "Run Eye Finder". This will compute the data stable regions relative to the clock edges and automatically configure the sampling positions for each bus channel. Note that for eye finder to properly measure the data stable regions, the target bus must have some traffic running across it, even if it consists of simple Idle control symbols.

Next, run the analyzer to capture some traffic. Triggering on "Anything" should be the default setting, so if this is your first run you do not need to change any trigger settings.

If the N4215A software is properly licensed, you can set up the tool set in the Workspace window, as shown in Figure 14.

Note the RapidIO icon in your "Toolsets" palette on the left side of the Workspace window. If you don't see it, you may not have licensed the software. If you didn't purchase the N4215A software with a new 16700 Series logic analysis system, you need to install it before licensing. Use "demo" as a license password for a free 30-day trial period.

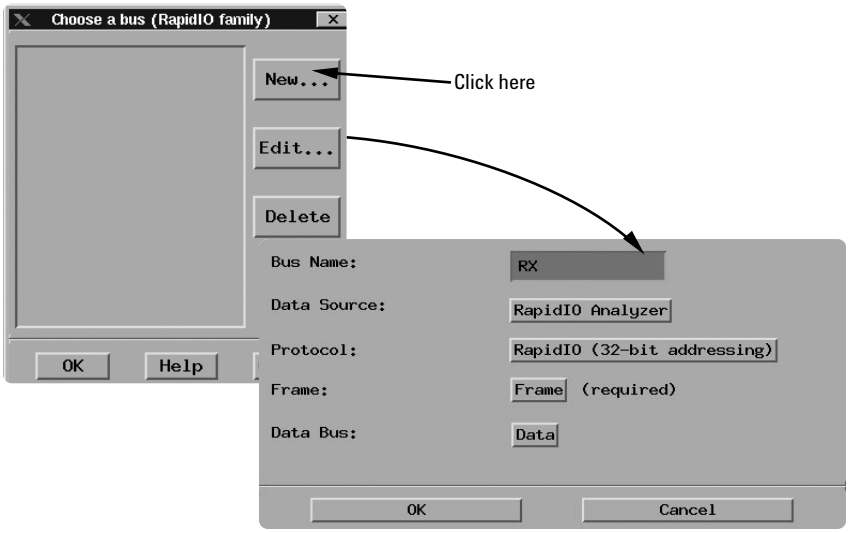


Figure 16. Bus selector setup

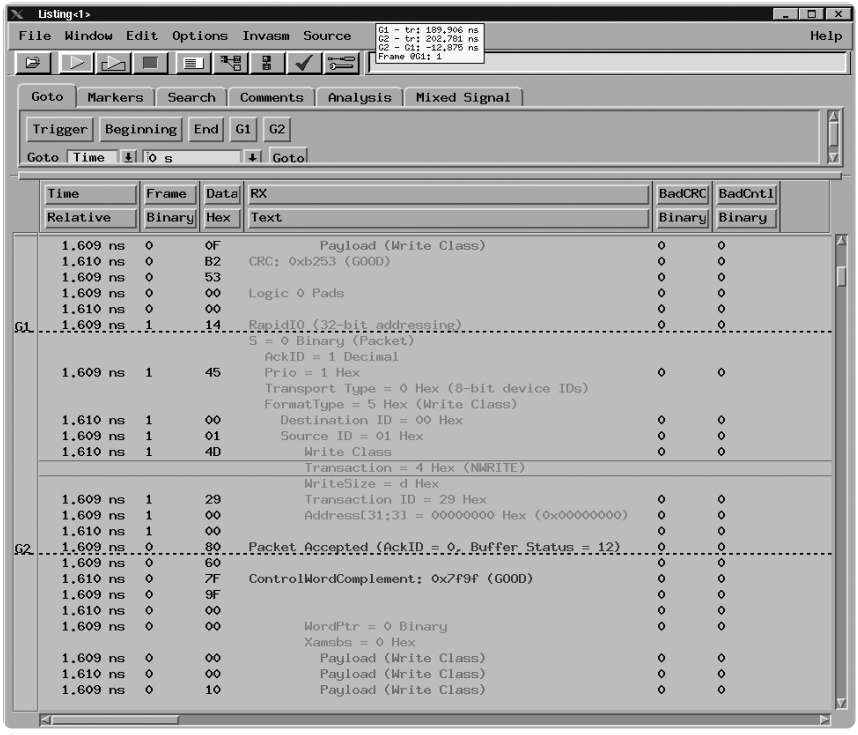


Figure 17. Listing window

Next, perform basic setup by clicking on the “RapidIO Tool” icon to bring up the setup menu. Clicking on the “Process Bus” icon (which says “No Bus Selected” by default, as shown in Figure 15) enables you to configure the bus definition. Clicking on the bus button brings up the bus selector.

Edit the bus so that the Frame signal is FRAME and the Data Bus is DATA (see Figure 16). Select your protocol based on your system addressing type (32, 48, or 64-bit addressing, not counting the extended address bits).

Click “OK” in the Bus Editor, “OK” in the Bus Selector, and “Apply” in the RapidIO Tool setup window, and go look at the Listing window shown in Figure 17.

On a state-by-state basis, the bus traffic is decoded. In the case shown in Figure 17, you can see an NWRITE packet being transmitted but temporarily paused to send a Packet Accepted control symbol. You can search for BadCRC=1 (for a bad packet CRC) or BadCntl=1 (for a bad Control-Word Complement) using the search capability of the Listing tool. You can also configure the tool to filter the display to show only control symbols, only packets, etc.

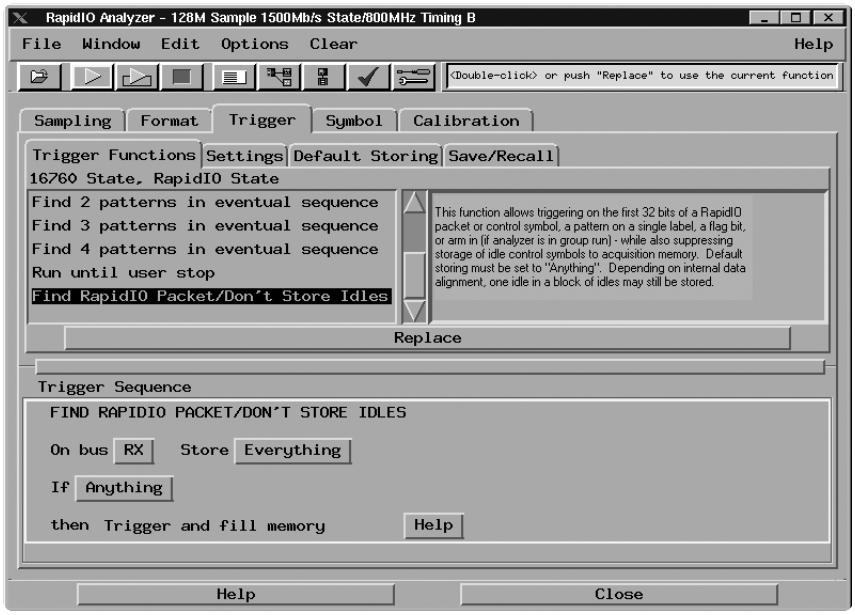


Figure 18. Trigger menu in logic analyzer setup window

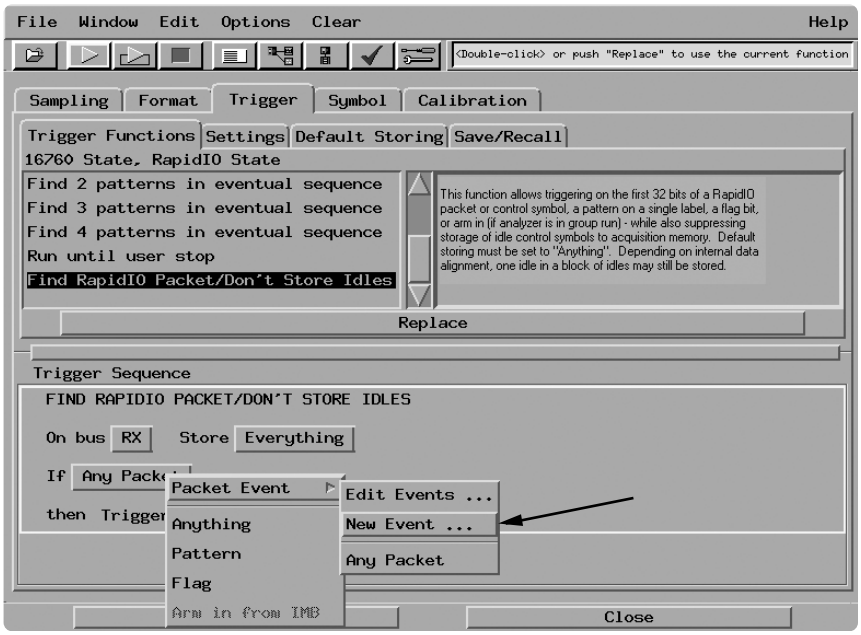


Figure 19. "New Event" button for setting triggers on specific packet or control symbol protocols

Real-time filtering of Idles and protocol triggering

The N4215A tool set also provides a 16760A trigger macro that performs real-time filtering of Idle control symbols. On an 8-bit bus, an Idle control symbol is actually a 4-byte (i.e., 4-clock) pattern, so store qualification (i.e., real-time filtering) is a challenge. But you can meet this challenge with the help of these tools.

Go back to the Trigger menu in the logic analyzer setup window, as shown in Figure 18.

Select the bus that you defined in the decode tool for the "On bus" button. On the button next to "Store", you can store "Everything", or "Everything but Idles". Now, if you have very sparse traffic, you won't waste 99 percent of that 64 Msample buffer on Idle time.

The trick for the bus analysis software becomes keeping track of how many Idles are not stored; if an Odd number of Idle symbols aren't stored, the "toggling" FRM bit won't toggle in the acquired data. That's not a problem for the N4215A tool set because a State Counts acquisition determines how many Idles are filtered out of the capture.

Next, from a protocol perspective, you can set triggers on specific packets and control symbols. At the "If Anything" button, select "New Event" (see Figure 19). You get the Event editor, where you can enter specific values into any of the fields in either packet or control symbol protocol.

Figure 20 shows a trigger setting for a Streaming Write packet. You can also specify Source and/or Destination device IDs by entering values into those fields. An “X” means you don’t care about the value in the field. Figure 21 shows a Control Symbol trigger for a Packet Not Accepted because of an Unexpected AckID.

These trigger settings are limited to the first 32 bits of packets and control symbols. Using an 8-bit transport type, you can trigger on any of the fields in the physical and transport layers of the RapidIO protocol.

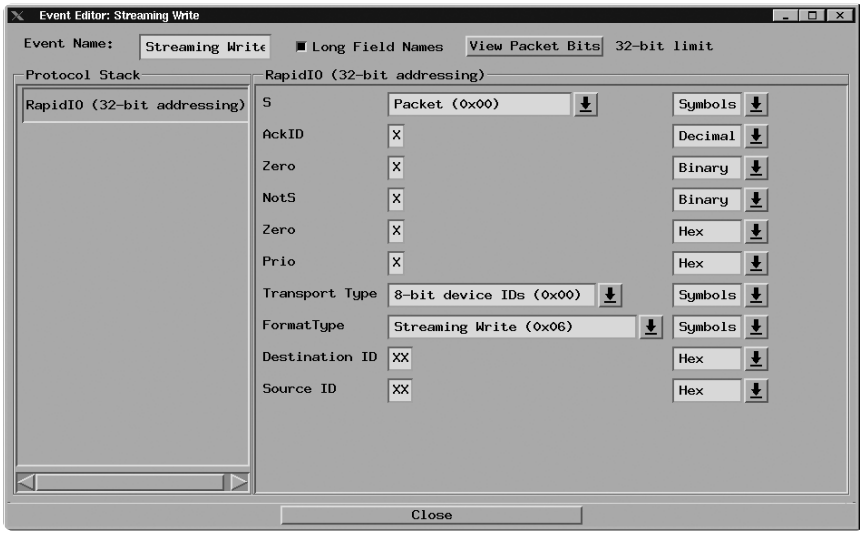


Figure 20. Trigger setting for a streaming write packet

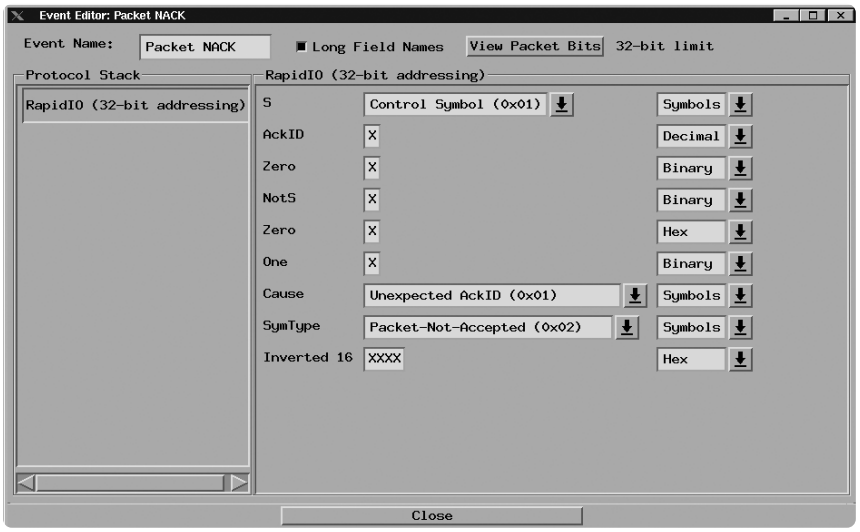


Figure 21. A Control Symbol trigger for a Packet Not Accepted because of an Unexpected AckID

Summary

This application note describes how to design in and use logic analysis for systems incorporating RapidIO buses. It explains the use of the E5387A differential soft touch probe adapter, the 16760A logic analyzer module, and the N4215A analysis tool set for RapidIO. These tools can help solve common problems, ranging from signal integrity issues to protocol and data flow problems.

Glossary

Compliant – able to move in the vertical (Z-axis) direction

DDR (Double Data Rate) — the result of clocking data on both rising and falling clock edges

Differential – the use of the difference in voltage between two signals to indicate transmission of a 1 or a 0

Eye diagram – a graphical display that indicates the quality of a digital data transmission

Eye finder – an Agilent measurement tool for automatically computing the optimal sampling positions on a parallel bus relative to the bus clock

Eye scan – an Agilent feature for capturing signal eye diagrams using a logic analyzer instead of an oscilloscope

Interconnect – a connection between two electronic devices

IP – Internet Protocol

Latency – the time delay between a request and its corresponding response

LVDS – low voltage differential signaling

Module – a plug-in card or set of cards connected together to operate as an acquisition device

Parallel bus – an electrical connection made with multiple channels and with an external clock

Probe loading – the adverse effect on a signal caused by connecting a probe

Probing – the connection of a measurement device to an electric signal

Protocol – the rules governing data communication on a standardized connection

RapidIO – A high-speed I/O interconnect developed by the RapidIO Trade Association (www.rapidio.org)

Reflections – electrical impulses transmitted on a wire when a signal bounces off a receiving device

Retention module – a mechanical device used to attach a soft touch probe to a circuit board, ensuring alignment between the circuit board pads and the spring pins of the probe

Serial bus – an electrical connection made with one or more channels with the clock embedded in the data stream

Signal integrity – the quality of data transmission, often characterized by an eye diagram

Related Literature

Publication Title	Publication Type	Publication Number
Agilent Technologies Digital Debug Solutions for RapidIO Buses	Technical Overview	5988-8439EN
The Agilent 16700 Series Logic Analysis Systems	Product Overview	5968-9661E
Processor and Bus Support for Agilent Technologies Logic Analyzers	Configuration Guide	5966-4365E, EUS
Designing High-Speed Digital Systems for Logic Analyzer Probing	Application Note	5988-2989EN
Saving Time with Multiple-Channel Signal Integrity Measurements	Application Note	5988-5409EN
E5387A and E 5390A Soft Touch Probe	Design Guide	E5387-97000

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