

# Logic Analyzer Specifications: How Much Timing Speed Do You Need?

Application Note 1582

## Introduction

When you buy a test instrument like an oscilloscope or a logic analyzer, you probably will inquire about the instrument's sampling rate. And you've probably been taught that the higher the sampling rate of the instrument, the better it is. However, this "truism" is not necessarily accurate for all conditions and all test instruments – faster doesn't always mean better. A logic analyzer's high-speed timing sample rate is a good example. The sample rate is only one factor that affects your measurements; memory depth is the other critical factor.

With logic analyzers, we normally sample at the conventional timing speed of the logic analyzer, but with the timing zoom feature

available on Agilent logic analyzers, you get a sampling rate of 4 GHz. You need to figure out what sampling rate you really need for the system you are working with, which is dependent on its timing speed.

This application note outlines the requirements for high-speed timing measurements. Sampling speed and memory depth both contribute to your ability to gain insights into your system activity. Faster sampling speed provides you with more details, and greater memory depth allows you to look at a larger quantity of data. The best instrument gives the longest capture time at high resolution. Additional features like View Scope and Eye Scan are great tools that provide additional insight into signal integrity issues.



## Timing zoom

Agilent's timing zoom samples at 8 to 10 times the conventional timing sample rate of the logic analyzer timing speed. This provides finer resolution and simultaneous state and timing measurements without double probing. The viewing area on the waveform display is adjustable from 100% pretrigger to 100% posttrigger. Timing zoom stores up to 64 K of memory depth with 250 ps of high-resolution data.

Figure 1 shows the timing zoom trace labeled "My Bus 1 (TZ)" in the logic analyzer's waveform display. A timing zoom trace provides more information. Data B8 and A8 were captured in timing zoom and not in the conventional timing trace. In this example, in conventional timing, we are sampling every 4 ns, yet with timing zoom we are sampling every 250 ps. In the 2-ns timing frame, timing zoom shows transitions on the bus that may be glitches in the system under test.

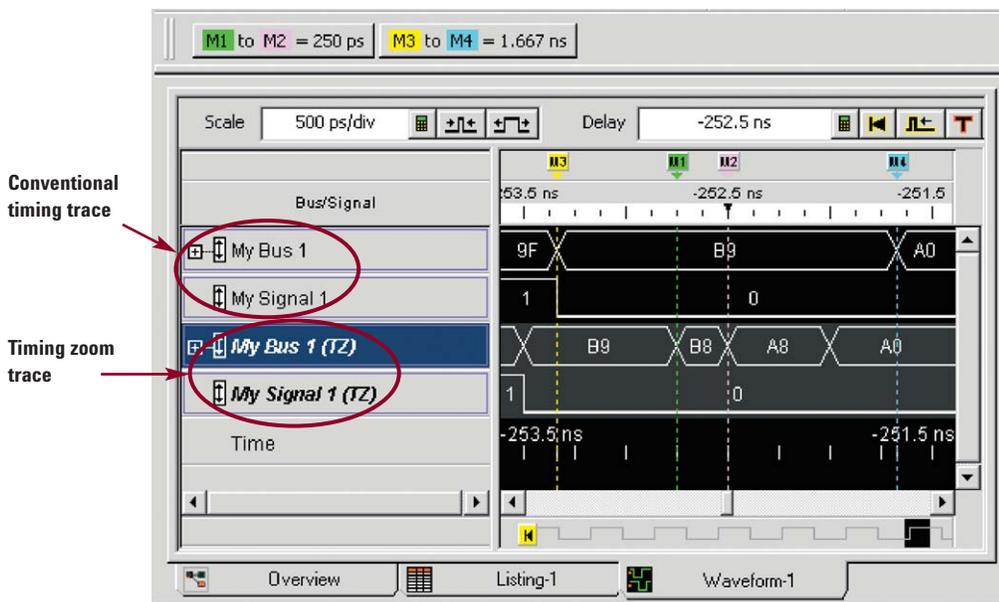


Figure 1. 4-GHz timing trace versus conventional timing trace

### Timing speed in relation to sampling rate

The Nyquist sampling theorem states that a signal must be sampled at a rate that is at least twice the highest frequency component to avoid the loss of information. For today's complex signals, higher sampling rates of 8x to 10x are recommended. 4 GHz timing zoom at 250 ps sample rate more than meets the timing sample requirements of most buses that can be measured with a logic analyzer.

You need to know the timing speed of the system under test to determine how much sampling you need.

Table 1 provides signal speed of your system with reference to the number of samples per clock period you can achieve with 4 GHz timing zoom. Thus, 4 GHz of timing zoom is more than sufficient for the majority of parallel bus measurements.

For further signal integrity checks and parametric measurements, you can use the View Scope

feature on Agilent 16800 and 16900 Series logic analyzers. View Scope allows accurate time correlation between the logic analyzer and oscilloscope traces.

Figure 2 shows an oscilloscope trace, glitch\_bit 7 of logic\_bus (TZ)[7] imported to the logic analyzer waveform window using the View Scope feature, the industry's first cost-effective solution that connects scope and logic-analyzer measurements using off-the-shelf BNC and LAN cables.

Signal speed	Signal clock period	4 GHz timing zoom (number of 250 ps samples per clock period)
100 MHz	10 ns	40
200 MHz	5 ns	20
300 MHz	3.33 ns	13.3
400 MHz	2.5 ns	10

Table 1. Signal speed in relation to the number of 250-ps samples per clock period

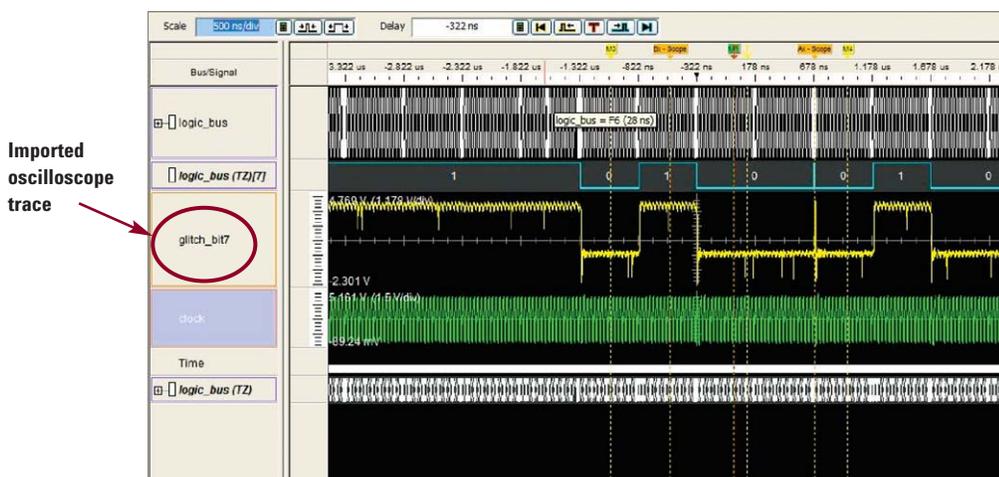


Figure 2. Using View Scope, you can see a deep oscilloscope trace integrated into the logic analyzer display.

## 64 K memory depth

Memory depth is the other key timing zoom specification that is really important. Timing zoom provides 64 K of memory depth with adjustable trigger position to give you insight into timing relationship between traces.

Figure 3 shows that for a conventional timing speed of 333 MHz, timing zoom is able to show 16  $\mu$ s of acquired time at 4 GHz, which is actually 8 times more than 16 K of memory depth with 2  $\mu$ s of acquired time. Note that you cannot trigger on timing zoom traces and have to rely on deep memory to store all the events, especially when a trigger event is not found. This will help to ease debugging work, and you will not lose valuable time taking multiple traces to find the problem.

## Conclusion

When you are deciding which logic analyzer to buy for debugging high-speed timing traces, you need to take into consideration the timing speed of the system under test and the memory depth of the logic analyzer you are considering. Faster doesn't necessarily mean better. For a 450-MHz signal, which is the maximum state speed of the logic analyzer, 4 GHz of timing zoom provides 10x sampling, and this is more than enough to provide insight into the timing relationships in your high-speed parallel buses. The best solution acquires the most measurement data at a high sample rate, giving you more information to find and solve your toughest debug challenges.

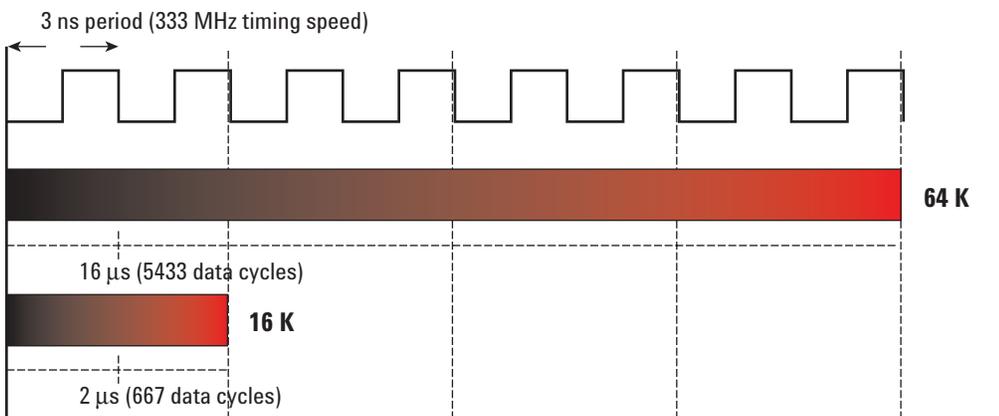


Figure 3. 64 K versus 16 K of memory depth in timing zoom

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