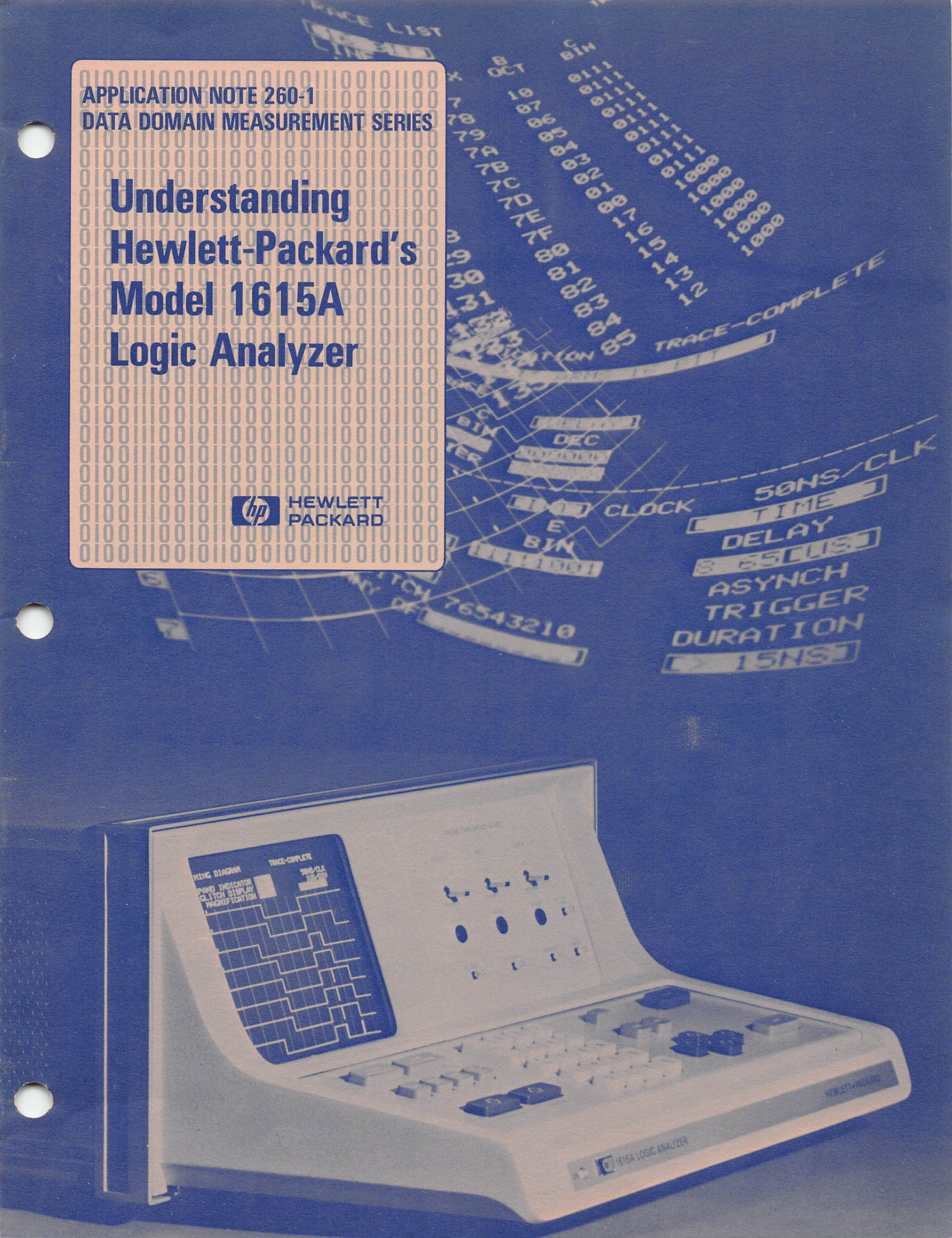
APPLICATION NOTE 260-1
DATA DOMAIN MEASUREMENT SERIES

Understanding Hewlett-Packard's Model 1615A Logic Analyzer

HEWLETT PACKARD




TRACE SPECIFICATION
TRACE ABORTED
TRACE
HEX
DEC
TRACE
CLOCK
DELAY
TRIGGER
DURATION
HEWLETT-PACKARD
1615A LOGIC ANALYZER

INTRODUCTION

The purpose of this application note is to provide familiarization with Hewlett-Packard's Model 1615A Logic Analyzer operation and to show how to perform digital system measurements using its powerful measurement set. The 1615A is truly a combination state and timing logic analyzer which can be formatted as a 24-bit state analyzer, an 8-bit timing analyzer, or a simultaneous 8-bit timing and 16-bit state analyzer. The analyzer incorporates a 24-bit wide, 256 word deep memory which operates with external or internal clocks to 20 MHz. Keyboard control and a menu concept make the analyzer exceptionally easy-to-use and understand.

THE MENU CONCEPT

Historically, instruments capable of complex measurements generally had an equal level of front panel complexity. By contrast, the 1615A is capable of highly complex measurements with a simple, easy-to-use keyboard (figure 1). The reduction of control complexity is achieved with a menu concept which displays, on-screen, the measurement parameters to be selected. Each menu, through the use of a movable cursor and a field select key, allows the setup of many measurement functions with minimum controls. In fact, only one key (Field Select) is used to make most of the measurement selections.

Data is entered by positioning a cursor, an alternating display of video and inverse video, using the four cursor positioning keys (figure 1).

If the cursor is positioned to a field enclosed by brackets (figure 2), such as Mode, Clock Slope, Logic Polarity, or Base, these selections are made with the Field Select key. If the cursor is positioned to a field without brackets, the entries are made using the other keys in the Entry block.

24-BIT MODE (STATE ANALYSIS)

With the 24-bit menu called, the analyzer is easily configured to monitor 24 lines of synchronous activity. With this menu, labels, clock slope, logic polarity, and bases are assigned to obtain the desired format. For example, with 16 bits connected to an address bus and 8 bits connected to a data bus, labels for the address and data buses can be assigned which allows each of these independent variables to be treated separately in terms of logic polarity and base (figure 2).

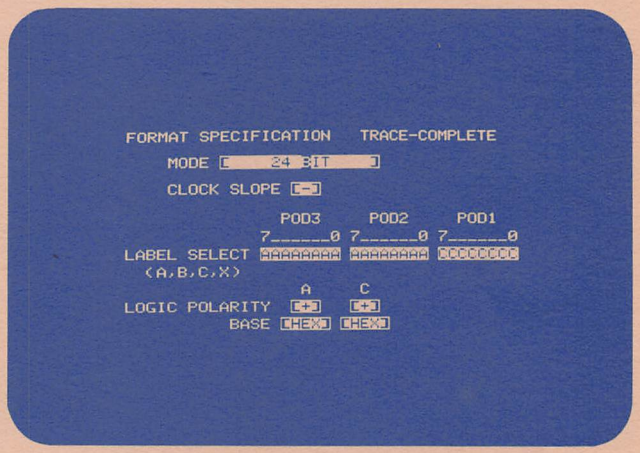


Figure 2. A Format Specification menu allows selection of Clock slope, assigns Labels to group data lines, and selects Logic Polarity and the numerical base to display and enter data.

The type of data and the area of program execution to be captured are entered in the Trace Specification menu (figure 3). A trigger point can be specified as any combination of the 24 inputs and is entered in the same format selected for display in the Format Specification menu (figure 2).

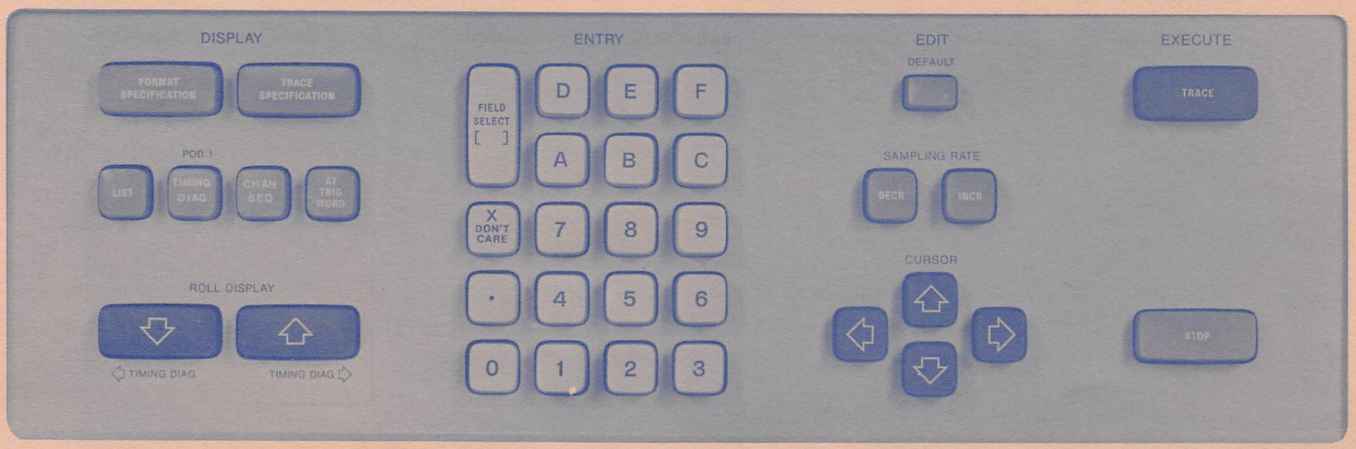


Figure 1. A logically arranged keyboard, divided into functional blocks with menus for setting up test parameters, allows entry of complex measurements with a minimum of controls.

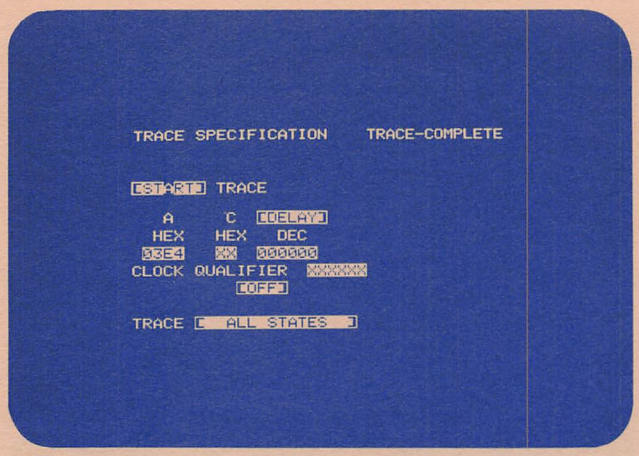


Figure 3. Trace Specification menu (resulting from the Format Specification in figure 2) shows the labels assigned (A and C) and the numerical base (HEX) in which to enter data. This specification defines that the Trace point will start data collection when address $03E4_{16}$ is recognized.

The trigger point may also be defined to start data collection or end data collection for viewing either positive or negative time information. A digital delay of up to 999 999 external clocks may also be selected to delay data collection to a desired point in program execution or for convenient paging through a program. Or, the digital delay field can be converted to an occurrence field to select the number of times the trigger word occurs, up to 999 999 times, before collecting data (figure 4) which allows triggering on the nth call of a subroutine or paging through loops.

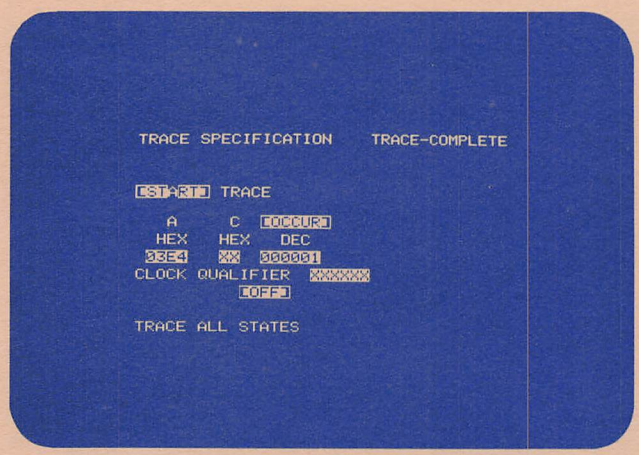


Figure 4. The Delay field (figure 3) may be converted to an occurrence field which specifies the number of times a trigger word must occur before data is collected.

The Clock Qualifier field (figure 5) refers to the six undisplayed clock qualifier inputs (Q0 thru Q5) on the clock probe. These qualifiers allow selection of the quality of data strobed into the 1615A's memory, such as only capturing data when a specific flag is set.

A second OR'ed qualifier field may also be added which allows combinations of qualifier patterns to

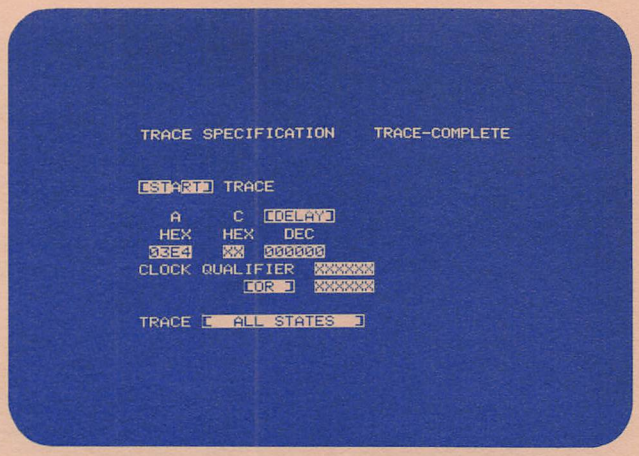


Figure 5. A Clock Qualifier field, six independent inputs on the clock probe, allows inputs in binary format to select the quality of data captured. This allows collection of only information of interest rather than just sequential activity.

be used. For example, to collect only I/O activity, two qualifier lines may be connected to the I/O read and write lines. Now, by setting the qualifier bits appropriately, only I/O read and write instructions are strobed into memory. Additionally, all states starting from a given qualified trigger point may be captured, or the All States field may be changed to Trigger Events which only allows trigger events plus any delay to be strobed into memory (figure 6). The Trigger Events plus Delay mode captures data at a specific point in program execution which allows you to view changes as the machine operates.

Figure 6. The Trace [ALL STATES] field may be switched to a [TRIGGER EVENTS] field which directs the 1615A to collect only trigger events plus any delay. This allows the capture of data a specific number of program steps after a trigger word to view changes in program execution.

Pressing the trace key now captures a listing (figure 7) of the activity to which the probes are connected with the display formatted in columns headed with the labels selected in the Format Specification. The brightened word in inverted video (columns labeled A and C) is the trigger word with 15 of the 256 words in memory displayed.

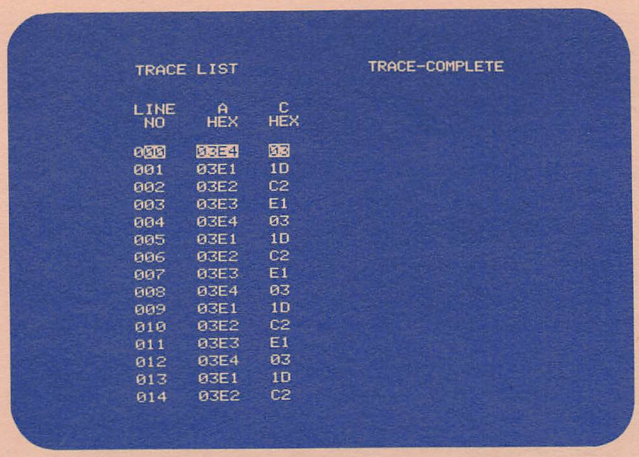


Figure 7. Trace List of data collected as defined by the Trace Specification in figure 3. The trigger word (if in memory) is displayed in inverted video (under Labels A and C) with 15 of the 256 words in memory displayed.

The words in memory may be moved through the display window by using the Roll keys. Or, a specific word can be directly accessed by placing the cursor in the Line Number field in inverse video and typing in the desired line number. The display can be restored to the trigger word by pressing the At Trigger Word key.

8-BIT MODE (TIMING ANALYSIS)

Timing analysis is accomplished in the 8-bit mode which is selected in the Format Specification menu (figure 8). The eight bits on Pod 1 are the only active inputs in this mode and are formatted with labels different than those in the 24-bit mode.

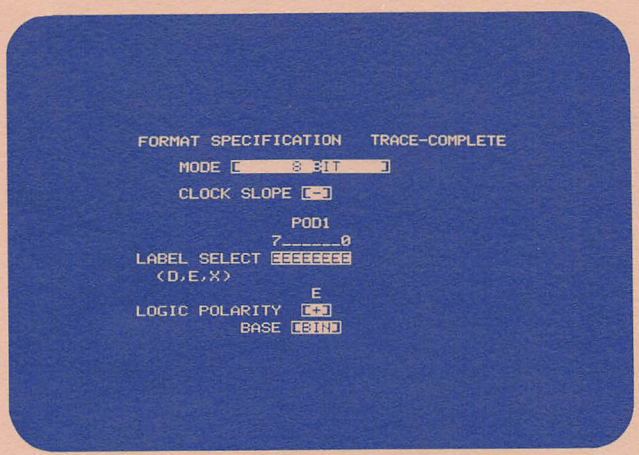


Figure 8. The Format Specification allows selection of an 8 BIT or Timing mode. The eight bits on Pod 1 are the only active inputs in this mode and are formatted with Labels different than those in the State mode.

The eight bit Trace Specification menu allows selection of either start or end modes of operation as well as internal or external clock source (figure 9). When internal clock is selected, the clock period is displayed on-screen. The clock period is not a menu controlled function but is controlled by two Sampling Period keys (figure 1) which increment or decrement the internal sampling clock.

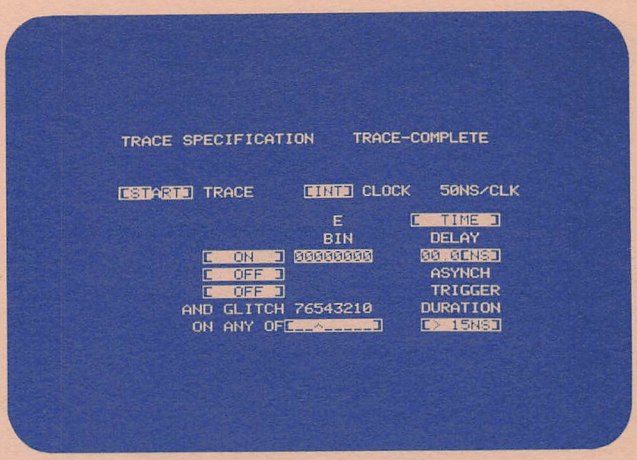


Figure 9. The eight bit Trace Specification menu allows you to select conditions under which you desire asynchronous data collected. In this example, the Analyzer will trigger when all eight lines have been low for at least 15 ns and a glitch is present on line 5.

Any 8-bit pattern may be used as a trigger word or the Boolean NOT of a pattern may be defined (figure 10). This NOT trigger condition is particularly useful when analyzing systems with status words. With this function, the analyzer will trigger on any deviation in a status word.

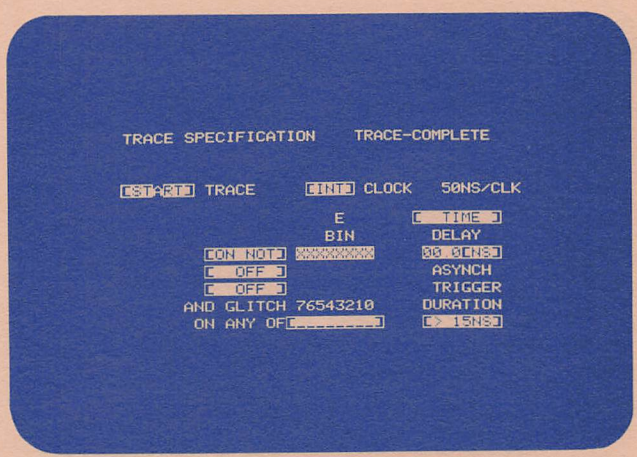


Figure 10. The eight bit trigger pattern is entered in the Trace Specification Menu and also allows the Boolean NOT of a pattern to be defined.

If the Boolean NOT trigger condition for a pattern of Don't Cares is specified, you have a trigger **never** condition. This may seem to be an odd trigger condition to specify, but it does have an application in the external clock mode. With the trigger **never** specification, the pattern on the eight lines can go through the entire 256 possible combinations without finding a trigger condition. Therefore, by using the end trace mode with an external clock, the analyzer passes data through the data acquisition network until a system crash occurs that stops the clock. The last 256 bytes of data before the crash are captured and can be viewed by pressing the Stop key.

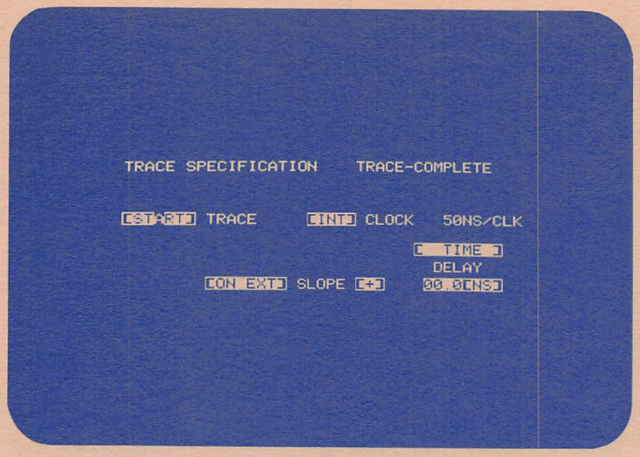


Figure 11. The [ON] field can be switched to an External trigger field which allows using the edge sensitive external trigger input on the clock pod as the trigger specification.

This [ON] field can be switched to an external trigger field with either the positive or negative going edge selected for strobing in data (figure 11). This external trigger input is on the clock pod and the trigger level is the threshold established for the clock pod.

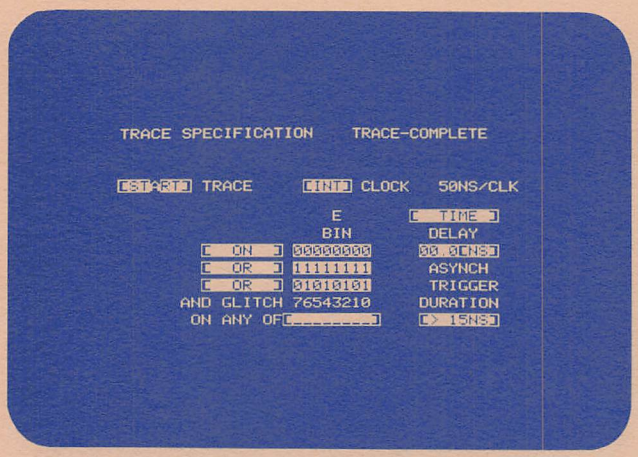


Figure 12. Up to three OR'ed fields may be defined to establish a trigger point which makes it possible to trigger on signals such as the Exclusive OR condition of a 2-bit pattern.

Up to three fields may be OR'ed to establish a trigger point (figure 12). This multiple OR'ed trigger field makes it possible to trigger on signals such as the Exclusive OR condition of a 2-bit pattern, or the first activity at specific I/O ports, or on the first interrupt from a multi-line interrupt driven system.

In addition to pattern triggering, glitch requirements can also be added to the trigger specification. The glitch can be defined to be on a particular channel or any one of a group of specified channels and may also be AND'ed with any trigger pattern. If it is desired to trigger only on a glitch, the pattern field can be filled with Don't Cares which means that the 1615A will capture data when a glitch occurs on a specified line. Since the glitch and pattern fields are AND'ed, it means that the glitch must be present "simultaneously" with the pattern to trigger the analyzer. Within the resolution of the 1615A, it can be stated that the glitch and pattern recognized as a trigger must exist in the same sampling clock period.

The 1615A defines a glitch as a transition in the direction of the last sample, or more generally, the second transition across threshold between sampling pulses. If a glitch occurs one or more sampling periods away from a data transition, it is displayed as a brightened vertical bar. If, however, a glitch is in the same period as a data transition, it is displayed as a brightened data transition (figure 13).

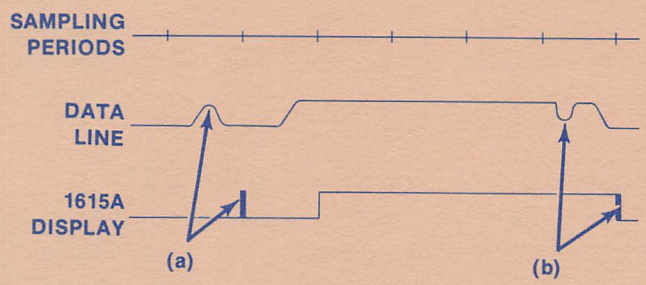


Figure 13. The 1615A displays a glitch that occurs between sample periods as a brightened vertical bar (a) and a glitch that occurs in the same period as a data transition is displayed as a brightened data transition (b).

The timing pattern trigger is truly asynchronous which means that the pattern does not have to exist at the time a sampling clock occurs. The only requirement is that the pattern must exist for the time specified in the asynchronous pattern duration field and then, on the next clock, data is strobed into memory. The asynchronous trigger duration field can be selected in 1, 2, 5 increments from 15 ns to 2 μs. All systems have transitory states caused by switching delays between lines (figure 14) which may represent false trigger points to the analyzer.

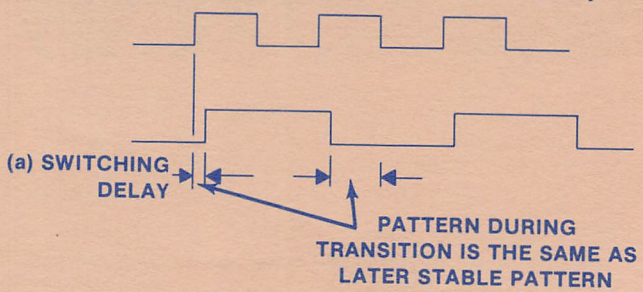


Figure 14. Because all systems have transitional states caused by switching delays (a), the 1615A has a trigger duration field which can be selected from 15 ns to 2 μs. This allows selection of the time a pattern must exist before the 1615A will capture data.

A system using components requiring only 20 ns setup time can respond to patterns that exist for only 20 ns. For these systems, a fast 15 ns asynchronous pattern duration matches the 1615A to the system under test. If, however, slower components are used or if a system runs at slower clock speeds with long logic paths, such as CMOS, 50 ns or 100 ns set up times are not unusual. For these slower systems, a 20 ns transient on the lines would be ignored by the system under test. Therefore, the asynchronous pattern duration field may be adjusted so that the 1615A also ignores narrow transient states. This adjustment allows the 1615A's asynchronous trigger capability to be matched to the system under test.

Time delay is available in the 8-bit mode (figure 9) which allows paging through asynchronous data just as digital delay is used to page through synchronous data. For example, if data are gathered in a start mode of operation using a 50 ns per clock sampling period, each of the graticule divisions represents one microsecond. This means that the 12 μs (12 divisions) of time following the selected trigger point is displayed on screen. By inserting 12 μs of delay in the time delay field, and retracing, the next 12 μs interval of time is displayed. If the End Trace mode of operation is selected, entering a time delay allows viewing of both positive and negative time around the pattern trigger (figure 15).

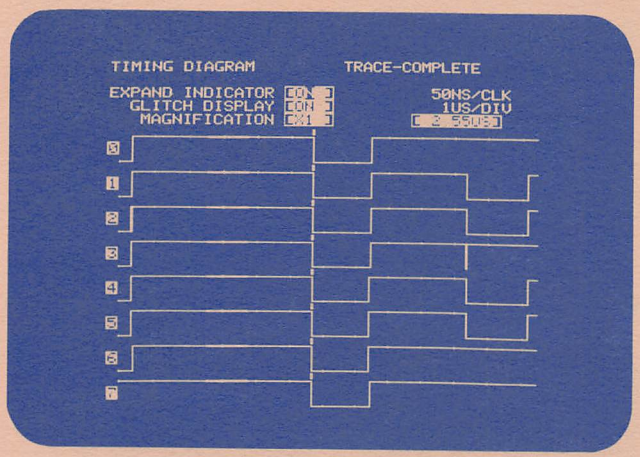


Figure 15. In an End Trace mode of operation a time delay may be entered to allow viewing both positive and negative time around a pattern trigger (brightened vertical dashed lines near center screen).

The maximum time delay that can be entered is 1 049 575 periods of the sampling clock. If delays greater than this equivalent number of sampling clocks are entered, a warning of Unallowed Value is displayed and no further activity is allowed in the menu until the error is corrected. Because the time increments are the period of the sampling clock, it is possible to enter numbers that have resolution far greater than one clock period but the analyzer will correct the input. For example, if the clock period is set to 100 ns per clock and a delay of 563 ns is entered in the delay field, the analyzer will automatically roundoff the entered number to the nearest whole clock period (600 ns) when any functional key is pressed. If the clock period were 50 ns/clock, 563 ns delay would roundoff to 550 ns.

External clock delay may also be selected (figure 16) which is in effect a digital delay that allows data collection to be delayed by known external events. For example, paging through handshake sequences or viewing the state of a series of control lines after the nth occurrence of an interrupt or data ready flag.

Figure 16. External Clock delay is also provided to allow data collection to be delayed by a known number of external events.

After all the Format and Trace Specification parameters are entered, pressing the Trace key causes the analyzer to look for its trigger point and, upon recognition, capture the asynchronous information which is displayed as a timing diagram (figure 17). At the top of the timing diagram display

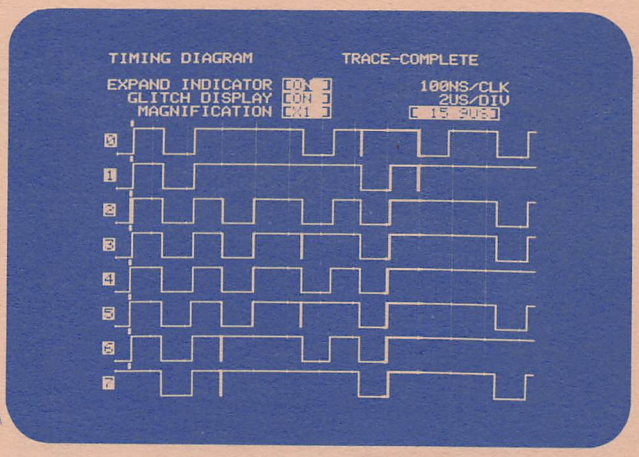


Figure 17. The captured data is presented as a timing display. Glitches are displayed as brightened edges and vertical bars. In addition, the sampling clock period and time per division are displayed. The trigger point is indicated at the left of the timing display by a short vertical bar on each timing line.

are two fields, Expand Indicator and Glitch Display which can be used to modify the display of captured information.

The 1615A always captures glitches which are displayed as intensified vertical bars or brightened edges on data transitions. If, however, the displayed glitches are not needed for the measurement, they may be turned off to reduce clutter. Displayed glitches may also be masked by the brightened Expand Indicator and for this reason the expand indicator may also be turned off.

The Expand Indicator is the brightened segment on the display that is just over one division long and it is moved to the desired on-screen location using the Roll keys. Now by positioning the cursor in the magnification field and pressing the Field Select key the display in the area of the expand indicator is magnified 10 times (figure 18).

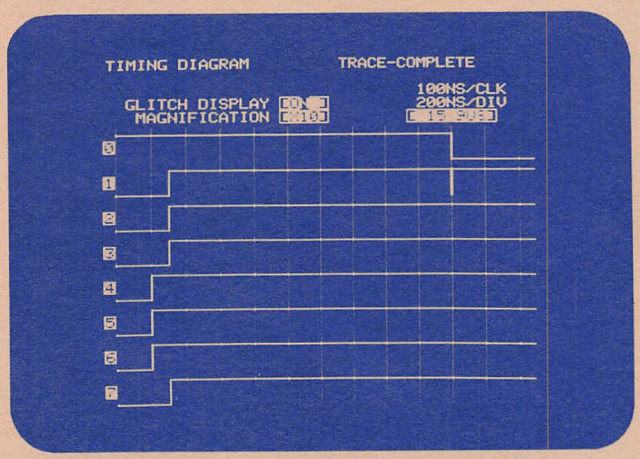
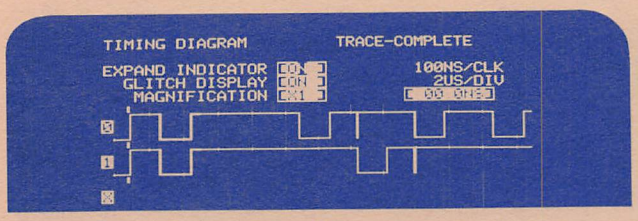
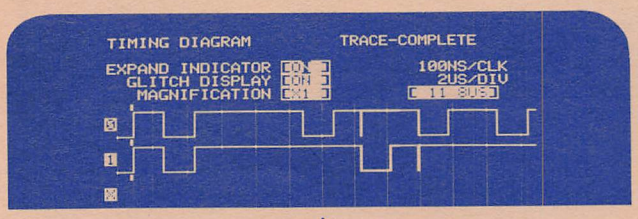


Figure 18. Increased visual resolution is provided with a times ten magnification capability. This example is a magnified display of the area covered by the expand indicator in figure 17. Also note that the time per division display also indicates the magnification.



a



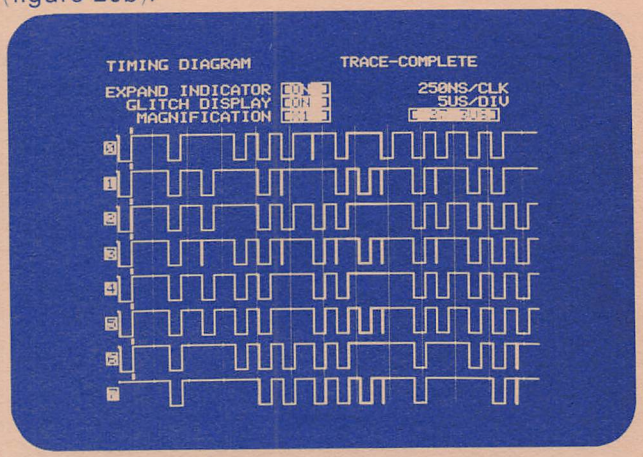
b

Figure 19. Relative time measurements can be made between points of interest on the timing display. In this example, the leading edge of the expand indicator (brightened trace segment) is positioned at the falling edge of a pulse on line 0 (a) and the relative time indicator zeroed; the expand indicator is then positioned on the falling edge of a pulse on line one with a direct readout of 11.8 μs (b) between these two edges.

Frequently, it is necessary to make time measurements between displayed events. A special direct readout time field allows these timing measurements to be made in conjunction with the Expand Indicator. For example, one edge of the expand indicator is aligned with one point of interest (figure 19a). The cursor may then be positioned in the field just below the time per division indication and the field zeroed with the Field Select key. Now, positioning the Expand Indicator to the next point of interest (figure 19b) provides a direct readout of time between the two points in the previously zeroed field.

TIMING AND LIST COMPARISON

Another capability of the 1615A is its ability to convert sampled data to a list in binary, hexadecimal, octal, or decimal format. The Expand Indicator is positioned to the area of interest (figure 20a) and when the list key is pressed a list of fifteen samples of data is decoded and displayed (figure 20b).



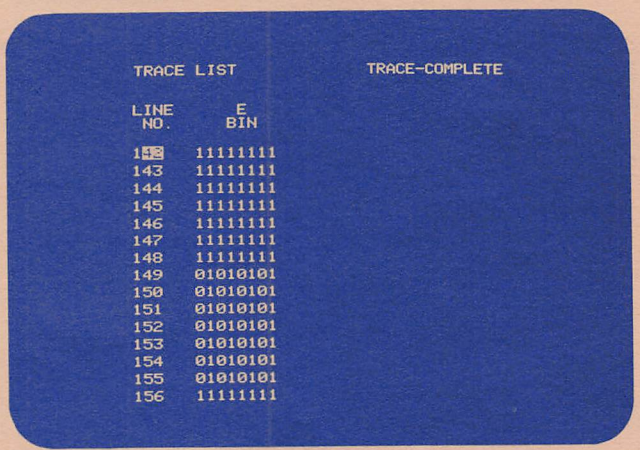


Figure 20. The timing diagram can be converted to a listing for convenient decoding by pressing the List key. When the Analyzer is in the Start display mode, the state listing corresponds to the first 15 samples of the intensified segment. When in the End display mode the state listing corresponds to the last 15 samples of the intensified segment.

The timing channels can be ordered in any desired sequence to aid interpretation of the measurement. At turn-on, the sequence is automatically set with zero at the top and seven at the bottom. However, to reorder the channels, simply press the channel sequence key which positions the cursor at the top of the channel number column. Now, the desired sequence may be typed in using the Entry keys (figure 21) or, if certain channels are not being used, they may be turned off by pressing Don't Care.

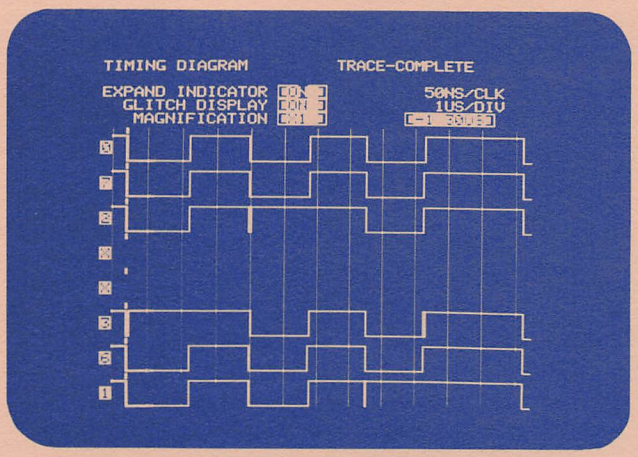


Figure 21. For maximum measurement flexibility and easy interpretation of the timing display, the display order of the timing channels may be organized in any desired sequence. For example, to allow closer examination of timing relationships between channels 0 and 7 they may be positioned next to each other.

STATE AND TIMING ANALYSIS

The 1615A also operates in a dual mode of operation where the 24 inputs are configured for a 16-bit state analyzer and an 8-bit timing analyzer operating simultaneously. The dual mode is selected in the Format Specification (figure 22) with the specification above the horizontal dashed line (near center screen) for the 16-bit state analysis and the specification below the line for the 8-bit timing machine. Labels, logic polarity, and bases are assigned to fit the desired measurement.

When the Trace Specification menu is called, triggering parameters may be entered to capture the desired information (figure 23). Triggering parameters for the 8-bit section remain unchanged from the 8-bit only mode. However, there are two subtle changes in the State menu: there is only one qualifier field because they are now split between the state and timing machines, and the Trigger Events mode is eliminated.

An additional field at the top of the specification menu allows configuration for any of four operating modes (figures 23 and 24).The interactive triggering capability in the dual mode makes it possible for the 16-bit state analyzer to provide trigger registration of the 8-bit timing analyzer to either trigger

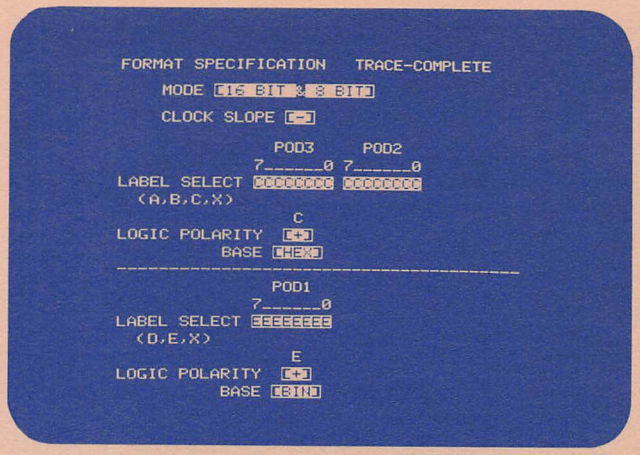


Figure 22. With the Format Specification menu called, the 1615A is configured for a dual mode of operation with 16 bits devoted to state analysis, Pods 2 and 3, and 8 bits for timing analysis, Pod 1.

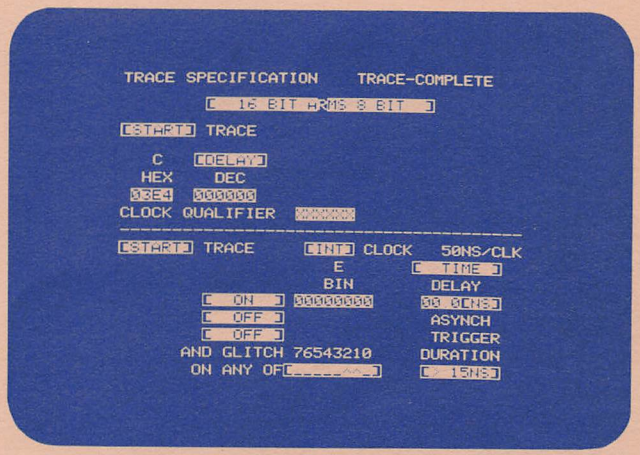


Figure 23. The desired interactive mode of operation and triggering parameters are selected in the Trace Specification menu. In this example, 16 Bit Arms 8 Bit is selected which, when the state machine recognizes its trigger word, will direct the 8-bit timing machine to search for its trigger word.

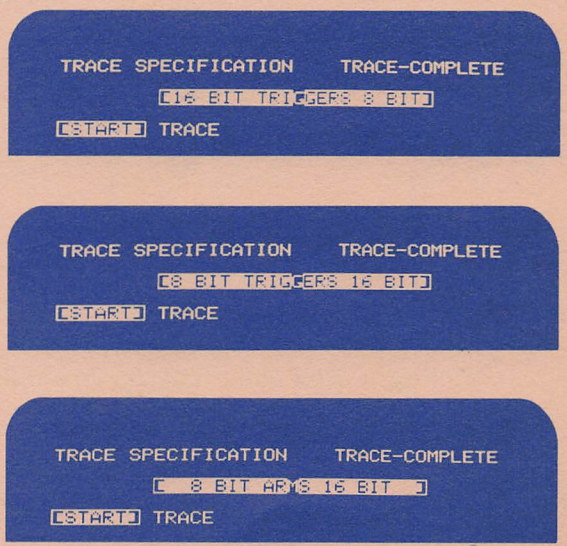


Figure 24. The analyzer may also be configured so that, upon trigger recognition, the 16 Bit machine Triggers the 8 Bit machine (a); the 8 Bit machine Triggers the 16 Bit machine (b); and the 8 Bit machine Arms the 16 Bit machine (c).

or arm the timing analyzer. In the ARMS mode the analyzer operates as a sequential trigger device. For example, if 16 BIT ARMS 8 BIT mode is selected, the trigger conditions established for the 16-bit operation must be recognized before the 8-bit analyzer can start looking for its trigger. The opposite is true with 8 BIT ARMS 16 BIT selected.

The ARMS modes are useful for:

1. Looking for a particular pattern on control lines after a specific point in program execution such as monitoring a status word for change only after completion of a bootstrap.

2. Achieving both digital and time delay in the same measurement.

Either the 16-bit or 8-bit analyzer can have absolute triggering control over the other in the 16 BIT TRIGGERS 8 BIT or 8 BIT TRIGGERS 16 BIT modes of operation. The triggering modes are particularly useful in relating asynchronous and synchronous activity within a system, such as:

1. Relating false interrupts to program execution.

2. Verifying that input lines are stable prior to reading an I/O port.

3. Verifying the status of control lines leading up to a subroutine call.

SUMMARY

The ability to configure the 1615A to accomplish State or Timing measurements with only keyboard entries allows this analyzer to be used to uncover both asynchronous or synchronous problems at the module or system levels.

For synchronous problems involving program execution, just configure the 1615A as a state analyzer with the following capabilities:

1. Inputs can be formatted to match the buses being monitored.

2. Coding in Hex, Octal, Decimal, or Binary.

3. Triggering on any pattern of the 24 inputs.

4. Digital delays of up to 999 999 clocks.

5. Occurrence triggering up to 999 999 events.

6. Dual OR'ed six-bit clock qualifiers.

7. Selective storage of ALL events, ONLY trigger events, or ONLY trigger events PLUS delay.

8. Clock speeds to 20 MHz and 256 word memory.

9. Positive or negative time capture of program execution.

For asynchronous malfunctions, handshake problems, or I/O measurement, simply configure the 1615A, with a few simple keystrokes, to a timing analyzer capable of:

1. Asynchronous pattern trigger with calibrated duration control.

2. Three OR'ed field triggering.

3. Boolean NOT trigger for status words.

4. External edge sensitive trigger.

5. Displaying glitches separately from data.

6. Glitch triggering.

7. Reordering displayed channels as desired.

8. Direct differential time readout.

9. Time or digital delay.

10. Timing diagram to coded list comparison.

11. Display expansion.

12. Positive or negative time capture.

And, if the area of concern involves the relationship of synchronous and asynchronous activity such as the source of system generated glitches or verification of status lines or I/O port data at a specific point in program execution, the dual mode of operation collects related synchronous and asynchronous data simultaneously in any one of four modes:

1. 16-bit state arms 8-bit timing.

2. 16-bit state triggers 8-bit timing.

3. 8-bit timing arms 16-bit state.

4. 8-bit timing triggers 16-bit state.

For More Information, Call Your Local HP Sales Office or, in U.S., East (301) 948-6370. Midwest (312) 255-9800. South (404) 955-1500. West (213) 877-1282. Or, Write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. —In Europe, Post Office Box 85, CH-1217 Meyrin 2, Geneva, Switzerland. —In Japan, YHP 1-59-1, Yoyogi, Shibuya-ku, Tokyo, 151. —In Canada, 6877 Goreway Drive, Mississauga, Ontario, L4V-IM8 Canada—

5952-2083

PRINTED IN U.S.A.