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Notes On Choke Network Design
AN-A001

Choke networks are sections of high frequency circuits whose purpose is to ensure that the correct DC operating point (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}) is supplied to an active device without allowing the DC supply circuitry to present an improper high frequency termination to that device. They serve a function that is complementary to that of DC blocking capacitors, which prevent the high frequency source and load resistances from improperly loading the DC supply circuitry while still passing the AC input and output signals.

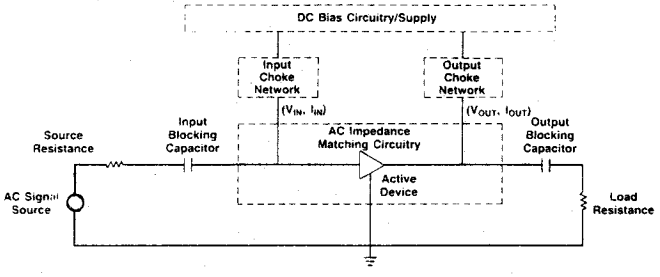

Figure 1. Typical high frequency amplifier.

Circuit designers often think of choke systems as DC pass networks that are simultaneously high frequency reject networks. This is an oversimplified definition that can lead the designer seriously astray. It assumes that the only function that the elements of the choke system serve is to keep the AC portion of the circuit separate from the DC portion. This need not be the case. Choke network elements can become significant parts of the high frequency impedance matching circuitry. They can also serve a major role in ensuring stable device operation. All these various aspects of performance need to be considered when designing choke networks.

DC Analysis Comes First

At DC, ideal capacitors act as open circuits and ideal inductors act as short circuits. Using these simplifications, a "reduced" DC schematic of the circuit being designed can be constructed and analyzed. Through correct component selection, the designer can then ensure that the proper voltages and currents are provided to both the input and the output of the active device. For this kind of analysis, choke networks on current controlled devices, such as the emitter-base junction of a bipolar transistor, usually reduce to short circuits at DC. Chokes for voltage controlled devices, such as the gate of a field effect transistor (FET), usually reduce to series resistors.

The associated resistance of molded inductors used as part of the choke system should be included in the DC analysis when significant. A DC power analysis should be made for each element to ensure that its dissipation rating is not exceeded. If the circuit is intended to operate over a broad temperature range, the temperature coefficients of all elements in the DC model should be considered and the DC analysis should be performed at hot and cold extremes as well as at "room temperature."

The Choke Network Should Next Be Analyzed At The Frequencies At Which The AC Portion Of The Circuit Is Intended To Operate.

If the choke network is intended to supply part of the high frequency impedance match, it must present the correct impedances throughout the operating frequency range of the circuit. If the choke network is not intended to play an active impedance matching role, then it should look like a large shunt impedance at circuit operating frequencies.

The design criterion in this latter case is that the impedance presented to the circuit by the choke system should be at least ten times the circuit impedance at the point of attachment. For current-controlled devices, or situations where large amounts of current are passing through the choke, this impedance is most often realized using either an inductor or a length of transmission line. The choice of a section of high-impedance transmission line whose electrical length is a quarter wavelength in the operating frequency band is particularly popular for relatively narrow-band circuits intended to operate above 1 GHz, the frequency at which such lines become short enough to be practically realized. Such a transmission line, when terminated with an AC short circuit in the operating frequency range, will present an impedance approaching that of an open circuit at the frequencies in the operating band while remaining "transparent" at DC.

For voltage-controlled devices, a resistor is more commonly used to realize this impedance. This resistor should be "backed up" by a capacitor providing a low-impedance path to ground at approximately 1 MHz (e.g., a 0.1 μf chip capacitor) to ensure that the resistor appears AC connected to ground when the 1 MHz impedance analysis is performed (see below). Configurations for both kinds of networks are shown in Fig. 2.

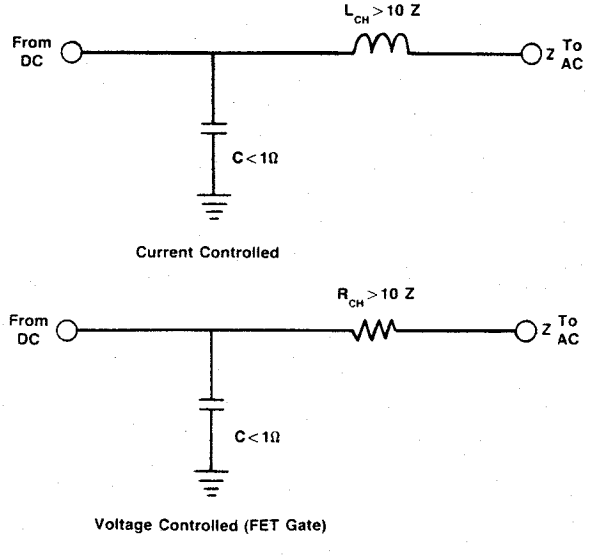

Figure 2. AC blocking/DC pass choke networks for current controlled and voltage controlled devices.

The Third Step Is To Perform An AC Analysis On The Choke Network Outside The Band Of Expected Operation.

This step is very important if stable operation of the active device is to be ensured, yet it is often overlooked by circuit designers. Most active devices used for high frequency amplification are only conditionally stable. Stability circles can be constructed for these devices using S parameter analysis, and from these circles terminations leading to stable operation can be determined. Such devices will remain "well behaved" as long as they are terminated with impedances from within these stable regions. Terminations from outside the regions of stability will result in oscillations and possible device destruction.

The terminations presented to the active device will, of course, come from the impedance presented by the AC matching circuitry combined in parallel with the impedance presented by the choke network. Proper terminations for stable operation must be maintained not only at the intended frequency of operation, but also at any frequency at which the active device is potentially unstable.

The junction capacitances and parasitic inductances associated with the physical layouts of high frequency amplifying devices, especially those capable of producing more than 100 mW of power, create transfer characteristics that allow most such devices to become superb parametric oscillators at 1-5 MHz unless they are properly terminated. In general, this means that for stable operation a resistive termination of between 10 and 20 ohms should be provided to both the input and the output of the active device at 1 MHz.

For current controlled devices, this is most often accomplished using a parallel combination of a "large" (impedance of greater than 100 ohms at 1 MHz) inductor and a 15-ohm resistor; for voltage-controlled devices, part of the resistance of the series feed resistor (R_{CH} in Fig. 2 above) can be used for this purpose. This low frequency termination section of the choke network should appear on the DC side of the AC blocking section discussed above. As with the higher frequency section, it is also followed by a low impedance path to ground, usually realized with a 1 μF capacitor.

Two words of caution: the resistive leg of the low frequency termination will be dissipating RF energy at 1-5 MHz and needs to have a high enough power rating to do so. Usually, a quarter-watt rating is sufficient, but for higher power devices a resistor with a higher power rating may be necessary. The 1 μF capacitor will also be passing this energy, and, consequently, high Q (low resistance) tantalum or electrolytic capacitors are frequently used for this element. Figure 3 shows typical circuitry resulting from these considerations.

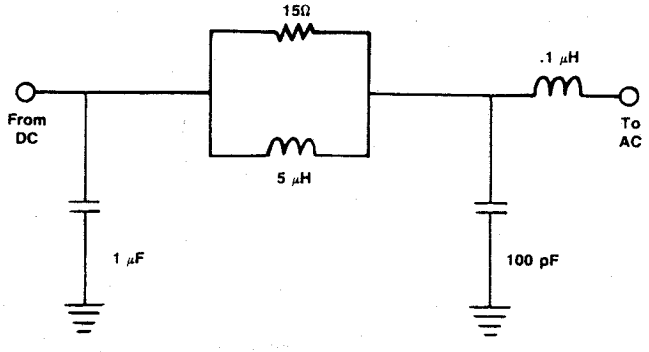

Figure 3. Typcial choke configuration for 1 GHz operation of a current controlled active device.

A similar scheme that uses the choke system to provide a resistive out of band load, and hence stabilize a potentially unstable FET, is shown in Fig. 4. In this circuit, bias is provided through a resistor whose value is selected to improve device stability. The optimum value of this resistor will, of course, vary with device S parameters, but values in the 25 to 100 ohm range are most common (too low a value will act too much like a short circuit; too large a value will act too much like an open circuit). This resistor is connected to the power supply through a section of transmission line that is AC grounded through a capacitor at a point one quarter wavelength at operating frequencies past the resistor. Thus, outside of the operating band the resistor forms a part of the circuit for stability, but in band the transmission line acts like an open circuit and "disconnects" the resistor from the circuit. Note that the order of the resistor and the transmission line is significant; a resistor followed by a length of transmission line has different impedances than a length of transmission line followed by a resistor. In general, the former will provide a better termination for stability.

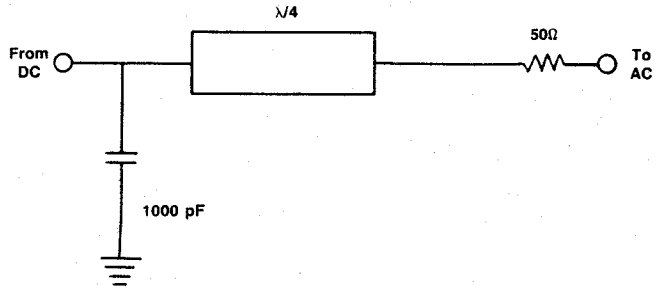

Figure 4. 4 GHz FET choke incorporating resistive stability termination.

An important special case of out of band terminations provided by the choke network occurs at those frequencies where loops in the choke network become resonant. At these frequencies a poorly designed choke network will often present impedances that cause the active device to become unstable. Many designers aggravate this problem by using multiple bypass capacitors in parallel for the low impedance path to ground. A resonant loop will be formed between each pair of capacitors, with the resonant frequency given by:

$$F = 1 / (2 \pi \sqrt{LC})$$

where F = the resonant frequency in Hz

L = the total inductance in the loop (sum of parasitic inductances, inductances due to path lengths, and intentional inductive elements) in Henrys

C = the total capacitance in the loop in Farads

At each resonant frequency, the effective termination provided by the choke network should be calculated, then compared to the stability circles of the active device at that frequency. The values of choke network elements should then be adjusted to ensure operation in the stable region. Keeping the number of loops in the choke system to a minimum by using only as many bypass capacitors as absolutely necessary, simplifies this process greatly and minimizes the risk of undesirable out of band terminations.

The Fourth Step Is To Analyze The Choke Network Under Dynamic (Transient) Conditions.

This step is particularly important when working with higher-power devices where relatively large currents are being switched and transient voltages of significant magnitude can be easily generated. The effect of most concern is that of a voltage being generated by a time-varying current through an inductor. This voltage, equal to L di/dt where L is the value of the inductor in henrys and di/dt is the rate of change of the current through the inductor in Amps per second, will add to the DC (steady state) bias voltage and the voltage generated by the AC signal, and can create voltage levels high enough to damage active device junctions by exceeding their maximum breakdown levels.

GaAs FETs are particularly susceptible to this failure mechanism because of their low breakdown voltages. A large capacitor must be provided to filter out these voltage peaks before they can reach the active device; electrolytics in the 68 μF range (RC time constant in the millisecond time range for a 50-ohm system) are typically used for this purpose. The use of such a capacitor is particularly important on test fixtures, where the wires used to connect the DC power supply to the fixture provide an inductive path which will generate voltage peaks every time the power supply is turned on or off.

A typical example helps illustrate this point. Suppose that a microwave test circuit is connected to a power supply through two feet of wire having an inductance of 20 nH/inch. A 50 pF chip capacitor is used to provide the high frequency ground at the end of the choke network. The transistor in the test circuit is capable of supplying 5 watts of CW power. It is biased Class A with 12 volts across the drain-source junction and operates at 33% efficiency. From the efficiency and the drain-source voltage, we can calculate the amount of current being switched: ΔI = (5 watts)/(12 volts $\times$ ⅓) = 1.25 Amps. The time to charge the 50 pF capacitor in a 50 ohm system is given by ΔT = 50 ohms $\times$ 50 pF = 2.5 ns. The inductance provided by the wires to the power supply is given by L = 20 nH/in $\times$ 24 in = 480 nH. The transient voltage generated at turn on can be approximated by (L $\times$ ΔI)/ΔT or (480 nH $\times$ 1.25 Amps)/2.5 ns = 240 volts. This is more than enough voltage to destroy most power FETs. If a 68 μF capacitor is used instead of the 50 pF described above, then the voltage spike drops to (480 nH $\times$ 1.25 Amps)/3.4 ms = .18 mV.

Some related problems occur whenever a transistor is used in pulsed operation. As the device turns on and off, the current through the choke networks will fluctuate, generating transient voltages which, if of enough magnitude, can damage device junctions. Voltages generated across an excessively high-inductance input choke used with a common emitter bipolar junction transistor, for example, will permanently degrade the emitter-base junction by continually driving it into reverse breakdown. Pulsed operation also requires the designer to use a high value capacitor on the transistor collector or drain feed for charge storage; without this capacitor the AC output waveform will exhibit significant pulse droop (decrease in output power versus time during the on cycle of the AC). The value of this capacitor will be a function of the pulse length and the droop that can be tolerated; values in excess of 100 μF are usual for pulses in the 100 μs time range (this value follows from the RC time constant of the circuit in question) with even larger values used for longer pulses. Low-Q capacitors and minimal associated inductance are also necessary for this application. Low input choke inductance is required in cases where fast rise times are important; at times, this requirement will force the designer to use chokes of low enough impedance that they become a significant part of the input impedance matching circuitry.

A few special "transient" effects that can occur if the power supply used to bias the device is abruptly switched on or off, rather than ramped up or down gradually, should be mentioned. Under these conditions, a poorly filtered power supply can internally generate unpredictable transients in addition to the L di/dt effects caused by current changing through the DC leads and choke system. Such transients are best investigated by direct measurement using a sampling oscilloscope.

The exact sequence of events, usually not well controlled when power supplies are abruptly switched on or off, can also influence device operation. Both excessive voltage at device junctions and unstable operation can result if the input of a device remains turned on while the output is in a state of flux. It is recommended that the input junction of the active device be turned off (set at zero volts if a bipolar, or at pinchoff if a GaAs FET) before bias is applied to or removed from the output of the device. If sparks are created in the switching process, such as often happens when leads are simply unplugged from the test fixture with the power supply left on, the impedance presented becomes completely indeterminate; since the spark is an energy source it may even appear to the active device as a negative terminating resistance—one of the best ways of designing an oscillator. The fact that device impedances are changing under transient conditions (the junctions act like voltage controlled capacitors) helps add to the possibility of oscillations occurring under these conditions.

A Few Additional Words About The Use Of Ferrite Beads And Cores In Choke Systems.

When properly used, ferrite is an excellent way of realizing high inductance in a choke system. The designer must keep in mind, however, that ferrite will also introduce loss and can create high frequency resonances that cause rather than solve stability problems. Ferrite material, like any other element in a choke system, should only be introduced to serve a specific purpose. The core material should be selected with a permeability suitable for the expected operation; while high permeability materials offer greater added inductance, they also have increased loss at higher frequencies. Since the core has loss it will dissipate power; the amount of power it must dissipate will limit its minimum physical size. Adding ferrite to the choke system can also lead to out of band terminatons that will result in unstable device behavior. In cases where it is suspected that this is happening, the impedance presented by the ferrite loaded choke system should be measured using a network analyzer and a stability analysis should be performed.

Figures 5 through 7 show some choke networks that incorporate the above considerations that are appropriate for several typical kinds of high frequency amplifiers. In none of these cases is the choke network intended to be part of the AC impedance matching network, which, for the sake of clarity, is omitted from the diagrams.

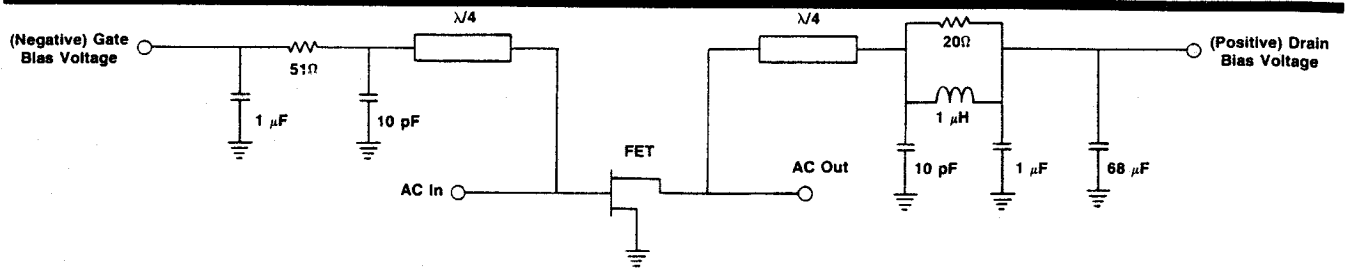

Figure 5. Typical 6 GHz GaAs FET choke network — IMFET.

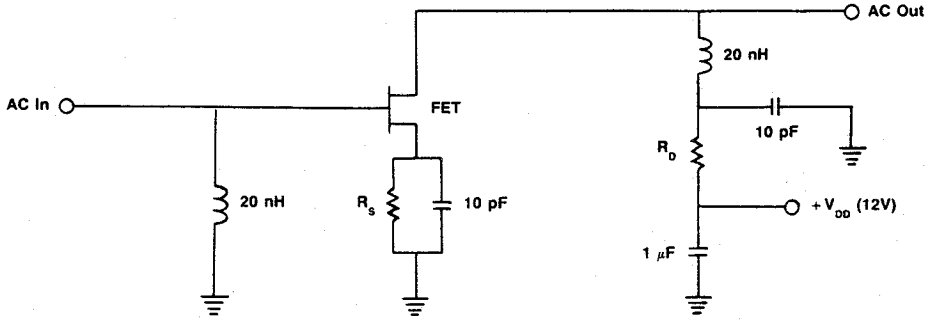

Figure 6. Typical 10 GHz small signal FET choke network using a single power supply (R_S and R_D selected to set bias).

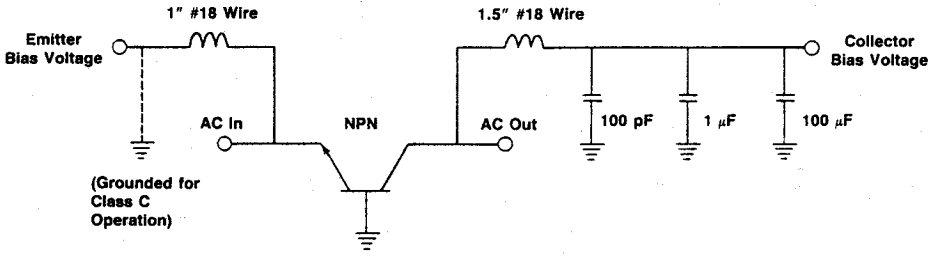

Figure 7. Typical L Band common base bipolar transistor choke network for high power Class C pulsed operation.

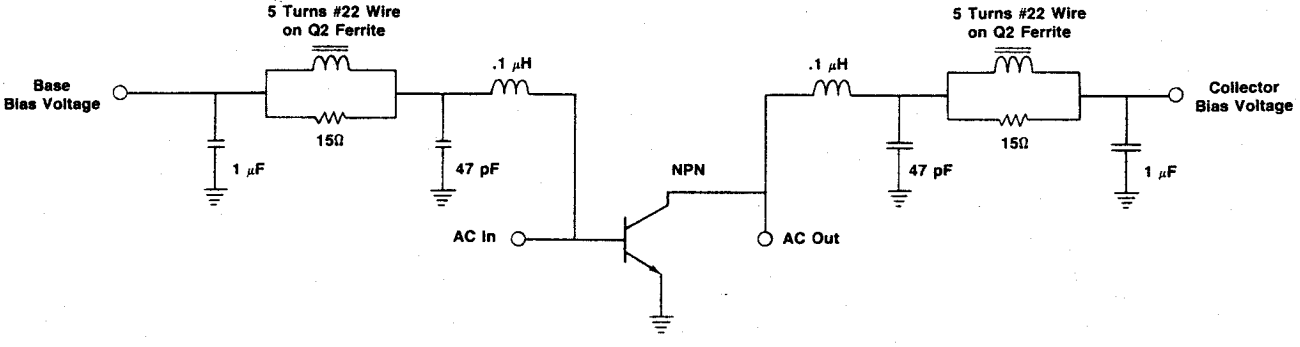

Figure 8. Typical 1 GHz common emitter bipolar transistor choke network.

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