HEWLETT PACKARD

AN-S004
A Broadband IF Amplifier Using MSA-0235 and MSA-0335

This application note describes the design and construction of a 10-1500 MHz, 20 dB gain, +10 dBm amplifier that uses two HP MODAMP™ MMICs. Such an amplifier could be used either as a general purpose gain block or as an IF amplifier in many high frequency systems.

Since the circuit is based on two 50Ω cascadable monolithic gain blocks, the "design" of the amplifier reduces to selecting the appropriate active devices and accurately simulating the parasitics that will necessarily be present in the finished amplifier.

The MSA-0335 was selected as the output device because of its output power (+10 dBm at $P_{1\ dB}$) and gain versus frequency characteristics (1 dB gain roll off at 1.8 GHz typical). The MSA-0235 was selected as the driver stage because it provides the same gain as the MSA-0335 at a lower current consumption and maintains a good gain versus frequency characteristic. In keeping with the premise that the design would be of a "quality commercial" nature, the package option selected was the "35," or micro-X. This glass sealed ceramic package offers good electrical performance at a reasonable price, and mounts flush with the PC board, simplifying construction. For a more economical design the "04" or "85" plastic, or "86" plastic surface mountable package option could be selected.

.1 μF ceramic capacitors provide DC isolation between stages and from the generator and load impedances. The capacitance value of these blocking capacitors determines the low frequency of operation of the amplifier; their associated parasitics limit high frequency performance and contribute to gain roll off versus frequency. The capacitors selected are high enough in value to provide a good low impedance path at the lower frequencies of operation. To minimize their impact on high frequency performance they must be used with their leads cut as short as possible. Some improvement in gain roll off versus frequency could be obtained by using chip capacitors with lower associated parasitic inductance instead, although typically chip capacitors would not be available in as high a capacitance value, and would, therefore, somewhat limit low frequency performance.

Sections of 50Ω transmission line complete the RF design. RT/Duroid 5870 was selected as the board material because its electrical and mechanical properties are appropriate for "quality commercial" design. Less expensive board materials, such as epoxy-glass (G10), could be used instead if price were more important than high frequency performance.

The DC bias circuitry consists of two ¼W resistors. The resistor values were selected to supply each MODAMP MMIC with its data sheet bias current when the amplifier is operated from a 12V power supply. Resistor values are calculated as follows:

$R_C = (V_{CC} - V_D)/I_D$

$= (12V - 5.5V)/35\ mA = 185\Omega$ for the MSA-0335

$= (12V - 5.5V)/25\ mA = 260\Omega$ for the MSA-0235

These values are rounded to standard values of 180Ω and 270Ω respectively in the final design. Total current draw for the finished amplifier turned out to be 63 mA when operated from a 12V supply. This bias approach has been shown to have excellent gain stability over temperature; less than 1.0 dB gain variation should be expected from this design over a temperature range of −25 to +65°C.

Although no chokes are used, the leads on the bias resistors are intentionally left long to add some inductance (10 to 20 nH) to the DC feed. Adding chokes of approximately .1 μH in series with the bias resistors would tend to improve the gain flatness versus frequency slightly; the chokes were omitted to demonstrate the performance that can be achieved with a "minimum component" amplifier realization. A feedthrough capacitor is used to terminate the bias resistors.

The entire amplifier schematic is shown in Figure 1. Note that only 8 components are needed: the 2 MSAs, 3 blocking capacitors, 2 resistors, and a feedthrough capacitor. Moreover, none of these components is particularly critical as to value, although keeping parasitics to a minimum when selecting components and assembling the amplifier will pay benefits in terms of the finished amplifier's high frequency performance. A photograph of the completed amplifier is shown in Figure 2.

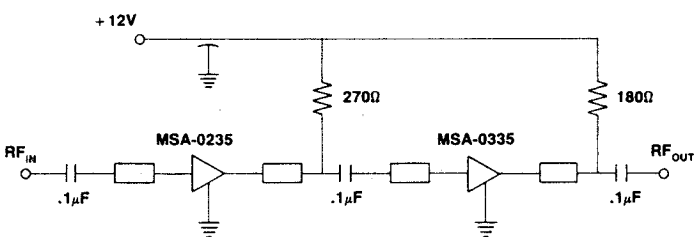

Figure 1. Schematic of 10-1500 MHz, 20 dB gain amplifier. All transmission lines are 50Ω.

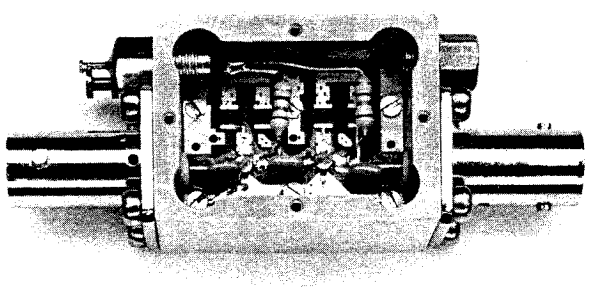

Figure 2. Completed Amplifier.

Figure 3 compares the predicted gain of the 2 stage cascade to that of the actual amplifier. The three curves shown represent an ideal cascade of two MSAs (CAS-S), a more realistic model including parasitics and the loading effects of the bias circuitry (CAS-P), and a measurement of an actual amplifier. Note that the model including parasitics agrees quite well with the measured performance, while the "ideal" cascade gives an overly optimistic estimation of both gain and gain roll off. The actual amplifier measured 21.5 ± 1.5 dB gain across 10 MHz to 1500 MHz, and still had about 10 dB of usable gain at 3 GHz.

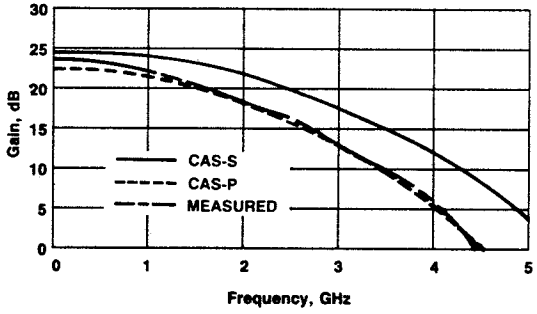

Figure 3. Gain.

Figure 4 compares the predictions of input match to what was actually achieved. Figure 5 does the same for output match. The return loss of both matches is typically better than 10 dB across the frequency of interest, indicating this structure is readily cascadable. The variations between predicted return loss and measured results is due primarily to the oversimplified model of the blocking capacitors used in the simulations.

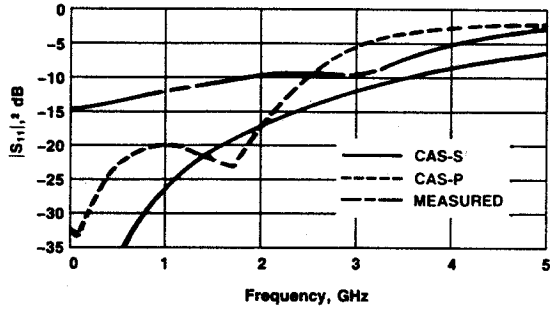

Figure 4. Input Match.

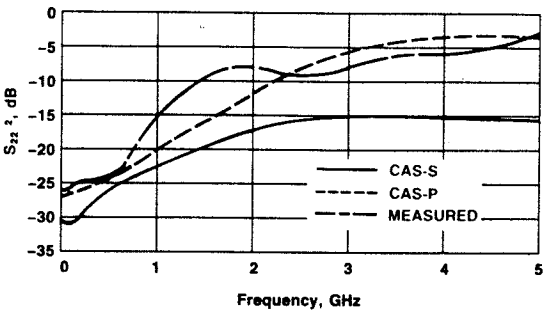

Figure 5. Output Match.

The harmonic content of the amplifier was also measured; this data is shown in Figure 6. Typically the second harmonic is more than 40 dB down and the third harmonic is more than 45 dB down. Saturation and compression were also measured; the results are shown in Figure 7. The saturated output was found to be about +13 dBm, and the $P_{1\,dB}$ agreed well with the data sheet value of +10 dBm.

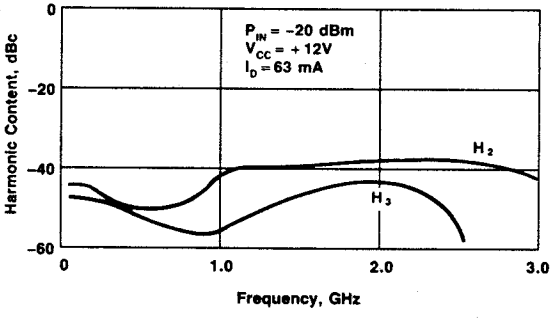

Figure 6. Second and Third Harmonic vs. Frequency.

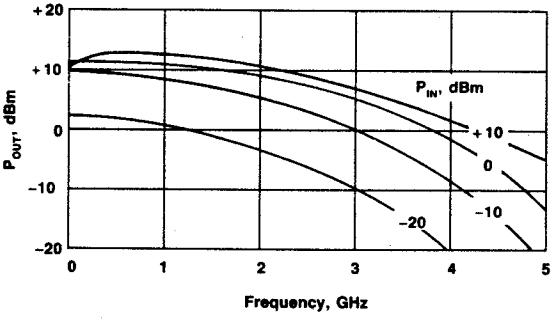

Figure 7. P_{OUT} Output vs. Frequency for various levels of P_{IN}.

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!CASCADE OF A0235 AND A0335

CKT
        MSUB    ER=2.56  H=32     T=1      RHO=1    RGH=0    !RT/Duroid 5870

!description of circuit including parasitics
        IND     1        2                L=.8             !connector transition
        SLC     2        3                L=1.2 C\100000   !.1uF + parasitic
        MLIN    3        4                W=95 L=100
        S2PA    4        5        51      MSA0235
        IND     51       0                L=.25            !common lead parasitic
        MLIN    5        6                W=95 L=150,
        RES     6        61               R=270            !bias R, stage 1
        IND     61       0                L\10             !L of bias R's lead
        SLC     6        7                L=1.2 C\100000   !.1uF + parasitic
        MLIN    7        8                W=95 L=150
        S2PB    8        9        91      MSA0335
        IND     91       0                L=.25            !common lead parasitic
        MLIN    9        10               W=95 L=100
        RES     10       101              R=180            !bias R, stage 2
        IND     101      0                L\20             !L of bias R's lead
        SLC     10       11               L=1.2 C\100000   !.1uF + parasitic
        IND     11       12               L=.8             !connector transition
        DEF2P   1        12               CAS-P

!description of ideal cascade
        S2PA    1        2        0       MSA0235
        S2PB    2        3        0       MSA0335
        DEF2P   1        3                CAS-S

FREQ
        STEP    .01      .05      .1
        SWEEP   .25      5        .25

OUT
        CAS-S   DB[S21]  GR1
        CAS-P   DB[S21]  GR1

        CAS-S   DB[S11]  GR2
        CAS-P   DB[S11]  GR2
        CAS-S   DB[S22]  GR3
        CAS-P   DB[S22]  GR3

OPT
        RANGE   .01      2
        CAS-P   DB[S21]<21
        CAS-P   DB[S21]>20

GRID
        RANGE   0        5        .25
        GR1     0        35       5
        GR2     0        -35      5
        GR3     0        -35      5
```

Table 1.

A Broadband IF Amplifier Using MSA-0235 and MSA-0335
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