HEWLETT® PACKARD

AN-S014
750-1250 MHz VCO

Introduction

The design and performance of two low-cost voltage-controlled oscillators (VCOs) for the 750 to 1250 MHz frequency range, intended for TV downconverter applications, are presented in this application note. Each VCO contains two active semiconductor devices, and both designs use the Hewlett-Packard AT-41411, as the oscillator. This semiconductor is an inexpensive low-noise silicon bipolar transistor in the SOT-143 surface-mountable package. For buffers, one version uses an HP AT-42086 medium-power bipolar transistor and the other uses an HP MSA-1104 silicon monolithic microwave integrated circuit. The varactor diode is a Siemens BB405B with a nominal capacitance range of 2-15 pF for a voltage range of 1-28 V. All devices in these designs are available in low-cost plastic packaging, and HP also offers a surface-mountable versions of the MSA-1104 that is designated MSA-1105.

Objectives

Both VCOs were designed for a minimum power output of +13 dBm over the specified frequency range. The specifications are summarized in Table 1.

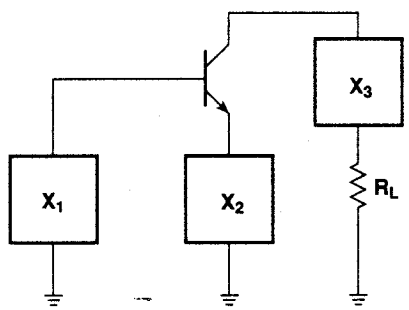
Table 1. VCO Specifications

Frequency:	750-1250 MHz
Power Output:	+13 dBm minimum
Power Variation vs Frequency:	± 1.5 dB
Supply Voltage:	+12 V ±0.1 V
Supply Current:	70 mA, maximum
Tuning Voltage:	1-23 V
Harmonics:	> -15 dBc

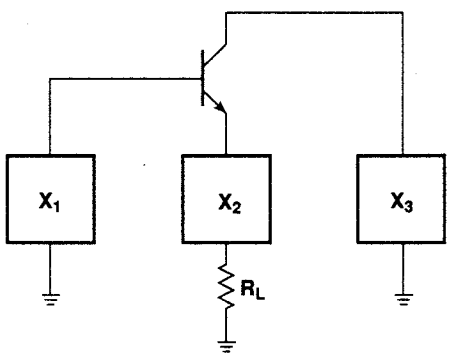
Oscillator Topologies

An oscillator may be designed using many different circuit configurations. For bipolar devices the oscillator can be visualized in a common-emitter, common-collector, or common-base configuration, with either series or shunt feedback used to produce oscillation. RF power from the oscillator can be obtained across a resistive load in series with any one of the reactive elements in a series-feedback oscillator or in parallel with a reactive element in a parallel-feedback oscillator. Several examples of basic oscillator circuits are shown in Figure 1. Additional information on oscillator topologies can be found in Reference 1.

Typical Oscillator Topologies Using Series Feedback

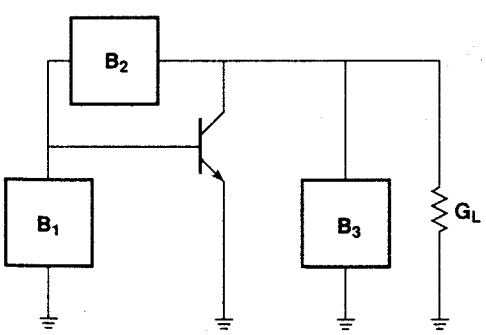


Power Taken From Collector

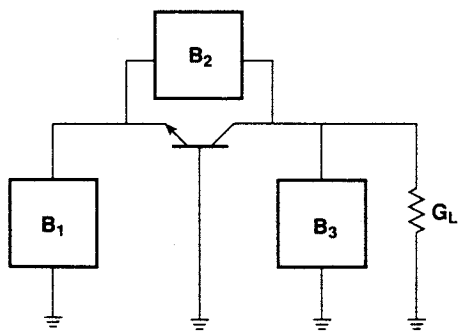


Power Taken From Emitter

Typical Oscillator Topologies Using Parallel Feedback



Power Taken Across Collector-Emitter



Power Taken Across Collector-Base

Figure 1.

Oscillator Design Procedures

For this oscillator we chose a common-collector design with series feedback. In the circuit the resonant frequency is established by the reactive network X_R, in series with the base of the transistor and ground. This configuration offers a simple biasing arrangement with only three resistors and no RF chokes required. The general oscillator topology is shown in Figure 2. In the case of this VCO design, the X_R network is tuned by a varactor diode in series with a microstripline section. X_{FB} provides series feedback, with a small value of capacitance connected between the transistor emitter and collector. The actual capacitance value will determine the lowest frequency at which the oscillator will reliably start. Power is delivered to the load via a matching network, X_m, at the emitter port.

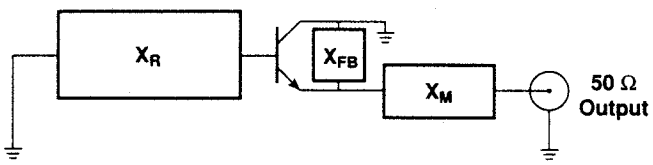


Figure 2. Common-Collector Oscillator

The design was analyzed using EEsof *Touchstone*®. Although *Touchstone* is strictly a linear analysis program it is capable of analyzing the circuits susceptibility to oscillation with various loads. With a device that is *not* unconditionally stable, i.e., k<1, it should be possible to terminate the S_{11} of the device in a matching network that will produce $|S_{22}|>1$. To simplify the oscillator design it is desirable to start with a device that is potentially unstable (k<1) at the frequency of operation. If k>1, then feedback must be introduced to make k<1. The feedback can be in the form of series feedback, i.e., in the common lead or shunt feedback from the output to the input port of the device.

Once a device with k<1 is achieved it is then a simple matter to load either the input port or the output port with the appropriate load to sustain oscillation at a particular frequency and into a particular load impedance. The equations are as follows:

For k<1 :

$\Gamma_G S_{11}' = 1$

$\Gamma_L S_{22}' = 1$

S_{11}' is the input reflection coefficient of the network under analysis with the output terminated in Γ_L. Likewise, S_{22}' is the output reflection coefficient with the input terminated in Γ_G.

Since the reflection coefficient of a passive matching network will be less than 1 the equations suggest that $|S_{11}'|$ must be greater than 1 to sustain oscillation. The equations also imply that if $|S_{11}'|$ is greater than 1, then $|S_{22}'|$ will also be greater than 1. In other words, if the device is oscillating at the input port it will also be oscillating at the output port and *vise versa*. Power will be delivered to the load that has the resistive termination. An extensive tutorial session on oscillator design is available in Reference 1.

Design Example 1:
Analysis as a 1-port network

Initially, the oscillator was analyzed as a 1-port network (Figure 3). The transistor, used in a common collector configuration is characterized as a two port network. The S_{11} of the device is terminated with a passive matching network that will produce $|S_{11osc}|$ of the oscillator >1. Examination of the equation shows that if we desire to match the output of the oscillator into a 50Ω load with less than a 1.02:1 VSWR (Γ=0.01) that $|S_{11osc}|$ should be greater than 100 for maximum power transfer. The load match can be optimized for a given output match over the required bandwidth.

A series-resonant circuit consisting of a microstripline resonator in series with a varactor diode was used to terminate S_{11} of the device. Initially the output of the device will be terminated in 50Ω. With the help of a computer optimization program such as *Touchstone* or Compact Software *SuperCompact*®, the values of the series resonant circuit can then be adjusted so that the network provides the necessary varactor voltage versus frequency relationship. The frequency at which $|S_{11osc}|$ peaks determines the frequency of oscillation. At this point in the design, it is only necessary that $|S_{11osc}|$ be greater than 1 over the desired band.

Next, the output matching network can be optimized to make $|S_{11osc}|$ as high as possible over the entire band as the varactor is tuned. In a narrow band situation it would not be difficult to obtain $|S_{11osc}|$ greater than 100, indicating a good match to 50Ω. However, since this is a broadband oscillator design it will be difficult to find by combining the matching network and a resonator circuit that will produce $|S_{11osc}|$ anywhere near that value. A good compromise is to establish $|S_{11osc}|$ in the range of 2 to 5 as the varactor is tuned over the band. Since power

® Touchstone is a registered trademark of EEsof
® Supercompact is a registered trademark of Compact Software, Inc.

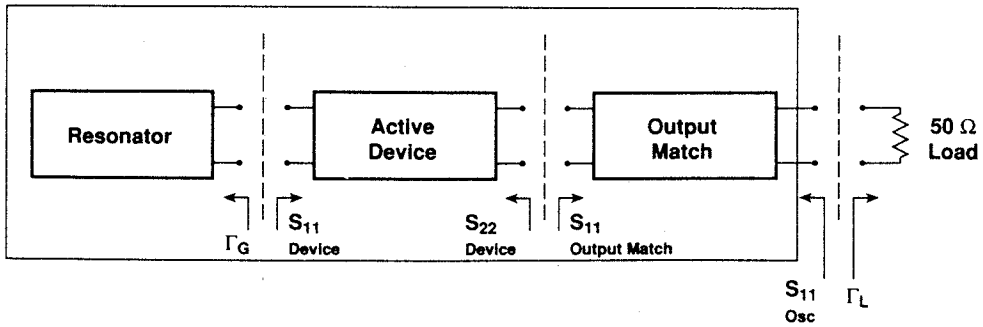


Figure 3. Block Diagram One-Port Oscillator Design

output of an oscillator typically drops as frequency is increased, it may be advantageous to design the network for better match at the higher frequencies in an attempt to flatten out the power versus frequency curve. A higher $|S_{11osc}|$ at the upper frequency will tend to offset the decline in gain of the active device.

A circuit file describing the circuit is shown in Figure 4. A schematic diagram is shown in Figure 5 and the computer results are shown in Table 2. The data indicates the value of the varactor required to maximize $|S_{11osc}|$ at three frequencies in the band. The output matching network consists of C1, C2 and R1. Choosing a C2 of 2.7 pF provides the appropriate amount of feedback to maintain k<1 over the entire bandwidth.

The design method described here merely predicts the frequency of oscillation. The design is approximate since only the small-signal S parameters are used in the analysis. To simulate power output or spectral purity including harmonic content and phase noise would require the use of a *SPICE*-based program, or one using the harmonic balance process.

Design Example 2, Analysis as a two-port network

Another method of designing an oscillator is the two-port method. The two-port network consists of the active device and the output matching network. The output matching network is designed such that S_{11}' of the two-port network is greater than 1 over the desired bandwidth. The external

Table 2. S_{11} vs. Frequency for Oscillator Shown in Fig. 5.

Frequency MHz	S_{11} Mag.	Angle	Varactor Capacitance
750	2.335	-142.1	14.2 pF
1000	2.520	-175.4	4.0 pF
1250	3.219	147.7	2.0 pF

```
DIM
      FREQ GHZ
      IND  NH
      CAP  PF
      LNG  IN
VAR
      C1\2.01006

CKT
      MSUB    ER=4.8   H=.031    T=.0007   RHO=1 RGH=O

      S2PA    1    2    3     A:\S_DATA\BIP\AT41411G.S2P

      SLC     2    0          L=.5 C=1000

      MLIN    1    5          W=.16  L=.85
      SRL     1    0          R=2200 L=1
      SRL     1    9          R=7500 L=1
      MLIN    9    21         W=.02  L=.37
      SLC     5    6          L=.5 C=1000
      MLIN    6    7          W=.02  L=.18
      SLC     7    0          L=5  C^C1
      SRL     7    8          R=10000 L=1
      SLC     8    0          L=1 C=1000

      MLIN    3    10         W=.10 L=.18
      SLC     10   0          L=.5  C=4.7
      MLIN    10   11         W=.10 L=.06
      SRL     11   0          R=62  L=.5
      SLC     11   12         L=1  C=10
      MLIN    12   13         W=.10    L=.10

      MLIN    3    20         W=.10    L=.10
      SLC     20   21         L=.5   C=2.7
      MLIN    21   2          W=.02    L=.07

      DEF1P   13               OSC
```

Figure 4. AT41411 Oscillator Circuit File

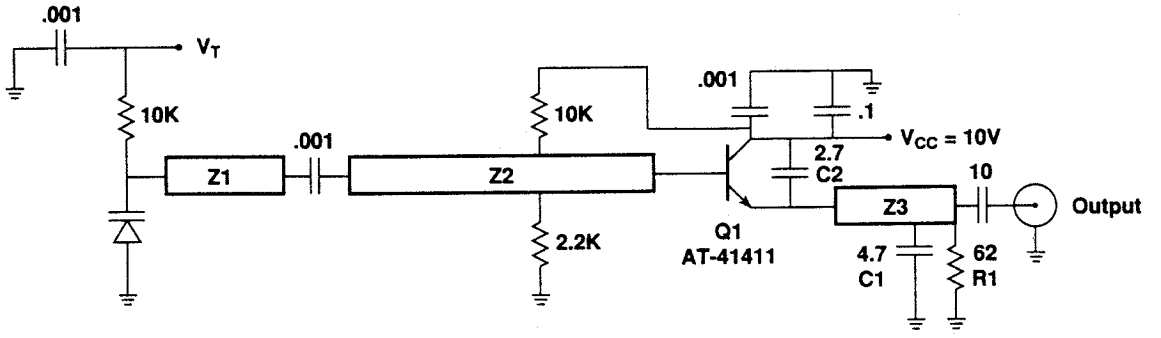


Figure 5. AT-41411 Oscillator Schematic Diagram

network Γ_G attached to the input of the two-port network is then designed to resonate with S_{11} of the network. The concept is shown in Figure 6.

To better understand what is involved with the two-port design approach, the VCO circuit described in Figure 5 will be analyzed as a two-port network. First, the resonator circuit (Figure 7) is detached from the rest of the circuit and analyzed. Next, the remaining circuitry (Figure 8) is analyzed separately over the same frequency range. The data in Table 3 reveals the change in Γ_G with varying varactor diode capacitance.

Compare this data with that shown in Table 4 for the rest of the circuit. For oscillation to start it is necessary for:

$$|\Gamma_G| > \frac{1}{|S_{11}|}$$

It is also necessary for:

$$\angle\Gamma_G = -\angle S_{11}$$

at the desired frequency of oscillation.

Note that both of these conditions are satisfied over the 750 to 1250 MHz frequency range as the varactor is tuned over its range.

A further analysis over a wider frequency range indicates that these conditions are met only at one frequency as the varactor is tuned. This precaution helps decrease the possibility of spurious oscillations.

Analyzing the circuit as a two-port network allows S_{21} to be calculated. S_{21} becomes very useful when cascading the oscillator with a buffer. It gives a good measure of the quality of the interstage matching network, and can be optimized for a particular gain flatness – a characteristic which is extremely useful for broadband voltage controlled oscillator applications.

It is clear that there exists an optimum output match that will produce an input reflection coefficient S_{11} of the two-port network which will best match the input resonator over the widest bandwidth. According to Vendelin,[1] choose a reflection coefficient of at least 1.2 to sustain oscillation. It is also good engineering practice to design for additional bandwidth on both sides of the desired band to allow for manufacturing tolerances.

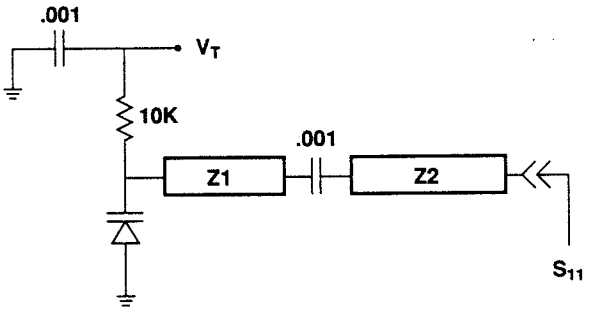


Figure 7. Resonator Circuit

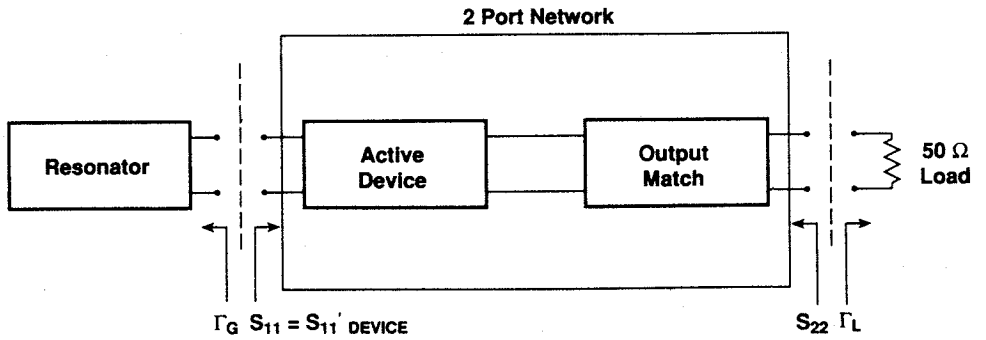


Figure 6. Block Diagram Two-Port Oscillator Design

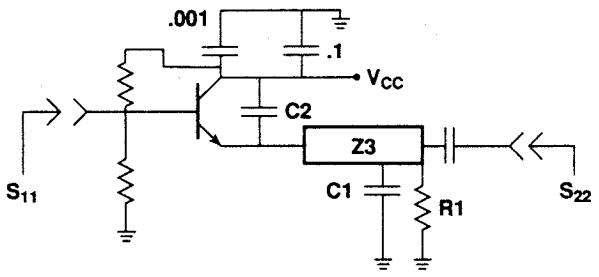


Figure 8. Schematic Diagram of Two-Port Oscillator

Table 3. Γ_G vs. Varactor Capacitance for Resonator Circuit Shown in Fig. 7.

Capacitance	Frequency MHz	Γ_G Magnitude	Angle	
14.0 pF	750	.951	39.0	*
	1000	.966	-73.3	
	1250	.986	-122.4	
3.7 pF	750	.994	-179.8	
	1000	.962	87.2	*
	1250	.969	-82.5	
1.7 pF	750	.991	-144.6	
	1000	.993	-173.9	
	1250	.981	137.5	*

The * indicates a resonant condition with the 2-port network shown in Fig. 6.

Design Example 3: Analysis of buffer configurations

To minimize pulling effects on the oscillator by the external load, it is advantageous to incorporate a buffer amplifier. The buffer amplifier provides greater power output than the oscillator stage would by itself, while contributing reverse isolation to minimize load pulling. The design of the necessary circuit is fairly straightforward. The steps are as follows:

1. Design the oscillator for operation over the desired bandwidth into a convenient impedance, i.e., 50Ω;
2. Design a buffer amplifier with input and output matched to 50Ω, giving careful attention to stability; and
3. Connect the two circuits and adjust the interstage matching networks for the desired response.

A block diagram of the complete VCO is shown in Figure 9.

The procedure for performing Step 1 in the design was described in the first design example. Steps 2 and 3 for either an MMIC or discrete transistor buffer, are covered in this section.

MMIC buffer

The simplest approach to a buffer amplifier is to use the MMIC. The HP MSA-1104 has a typical gain of 12 dB with 1 dB gain compression point (P_{1dB}) of greater than +17 dBm. The low input and output VSWR of the MSA-1104 combined with14 dB of reverse isolation makes it an ideal buffer for the oscillator stage.

The basic VCO is analyzed as a two-port and cascaded with the MSA-1104 stage. The results of the simulation are shown in Table 5. The circuit file is shown in Figure 10 and a schematic diagram in Figure 11. The two-port network was optimized for

Table 4. Computer Simulation for Two-port Oscillator Shown in Fig. 8.

Frequency MHz	S_{11} Magnitude	Angle	S_{21} dB
700	1.45	-34.5	8.37
750	1.53	-39.3	8.92
1000	1.85	-86.8	10.85
1250	1.52	-137.5	9.37
1300	1.39	-148.2	8.59

Table 5. Computer Simulation of Two-port Oscillator Using the AT-41411 and MSA-1104

Frequency MHz	S_{11} Mag.	Angle	S_{22} Mag.	Angle	S_{21} dB
700	1.32	-31.1	0.54	-133.1	19.7
750	1.35	-34.3	0.55	-150.6	19.9
1000	1.82	-61.5	0.41	137.3	21.2
1250	2.63	-130.6	0.71	139.4	21.6
1300	2.19	-151.5	0.83	120.2	19.3

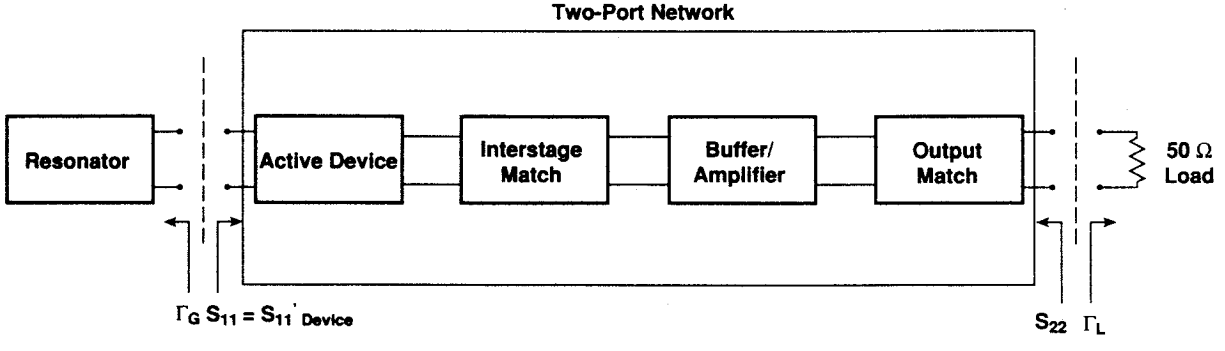


Figure 9. Block Diagram Buffered VCO Design

```
DIM
      FREQ GHZ
      IND  NH
      CAP  PF
      LNG  IN

CKT
      MSUB    ER=4.8   H=.031  T=.0007      RHO=1 RGH=O
      TAND  TAND=.003

      S2PA    1    2    3        A:\S_DATA\BIP\AT41411G.S2P

      SLC     2    0             L=.5 C=1000

      MLIN    3    10            W=.10 L=.15
      SLC     10   0             L=.5 C\2.46985
      MLIN    10   11            W=.10 L=.06
      SRL     11   0             R=62 L=.5
      SLC     11   12            L=.5 C\11.76285
      MLIN    12   13            W=.10 L=.10

      MLIN    3    20            W=.10 L=.10
      SLC     20   21            L=.5 C=4.7
      MLIN    21   2             W=.02 L=.07

      MLIN    13   30            W=.05 L=.5
      S2PB    30   31   32       A:\S_DATA\MODAMP\MSA1104.S2P
      MLIN    32   40            W=.020   L=.020
      MLIN    32   41            W=.020   L=.020
      VIA     40    0            D1=.025 D2=.025   H=.031   T=.0007
      VIA     41    0            D1=.025 D2=.025   H=.031   T=.0007
      MLIN    31   33            W=.05 L=.2
      IND     31   36            L=330
      SLC     36    0            L=.5 C=1000
      SLC     33   34            L=.5 C=1000
      MLIN    34   35            W=.05 L=.2

      DEF2P 1 35 OSC
```

Figure 10. AT-41411/MSA-1104 VCO Circuit File

Table 6. Performance of VCO using AT-41411 oscillator and MSA-1104 buffer

Tuning Voltage V_t	Freq. MHz	Pwr Output dBm	2nd Harm. Level -dBc
0	670	+16.7	-10
1	720	+15.9	-14
5	830	+16.6	-25
10	980	+17.0	>-35
14	1000	+16.3	-
20	1240	+13.2	-
22	1280	+12.3	-
24	1310	+11.9	-
26	1345	+11.5	-
33	1390	+10.5	-

Table 7. Computer Simulation of Two-port Oscillator Using the AT-41411 and AT-42086

Frequency	S_{11}		S_{22}		S_{21}
MHz	Mag.	Angle	Mag.	Angle	dB
700	1.74	-31.8	0.65	-6.7	24.1
750	1.90	-39.0	0.70	-13.9	25.4
1000	1.77	-102.1	0.67	-43.8	27.1
1250	1.44	-137.9	0.76	-107.1	25.5
1300	1.35	-149.3	0.64	-128.6	24.3

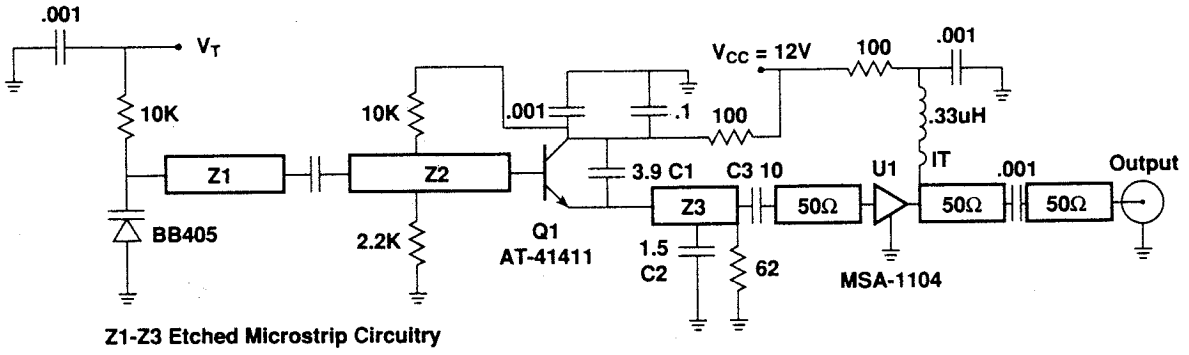


Figure 11. Schematic Diagram VCO with MMIC Buffer

gain, gain flatness, and input reflection coefficient over the tuning range. Note that $|S_{11}|$ is greater than 1.2 over the desired bandwidth which means that the resonator circuit discussed earlier will resonate properly. The shunt feedback capacitor C1 has a major effect on $|S_{11}|$ and on the circuit's ability to oscillate at lower frequencies. According to the simulation 4.7 pF was optimum for C1. Too high a capacitance for C1 lowers high frequency gain, and hence, power output. Actual measurements indicate that 3.9 pF yields dependable oscillator startup at 750 MHz with minor degradation in high frequency performance. It was found empirically that the matching network consisting of C2 at 1.5 pF and C3 at 10 pF offers the highest power output over the frequency range. Note that these are very close to the 2.5 pF and 11.8 pF values produced by the computer simulation program.

An indication of tuning bandwidth may be obtained by reviewing the angle of S_{11} in the computer simulation data. As the feedback capacitor and the matching elements are varied for the desired gain and low-frequency startup, the tuning bandwidth will change.

Actual VCO performance is shown in Table 6. Power output measured +13.5 dBm to +16.8 dBm from 740 MHz to 1240 MHz. The required tuning voltage is 1 to 20 V. If the tuning voltage is varied from 0 to 33 V, the VCO actually tunes from 670 MHz to 1390 MHz. Worst case inband harmonics are -14 dBc.

Bipolar transistor buffer

An alternative to the MMIC buffer is to use a discrete bipolar transistor with appropriate matching networks to obtain relatively constant power output across the band. The Avantek AT-42086 was chosen for its moderate power output and fairly high gain.

The bipolar transistor buffer is designed to be unconditionally stable and to have broadband gain from 750 to 1250 MHz as measured in a 50Ω system. The buffer is then connected to the oscillator stage, as described in Figure 5. The interstage matching network and feedback capacitor are then optimized for flat gain over the band while still ensuring that $|S_{11}|$ is greater than 1.2. It is also important to analyze the ratio of the reflection angle at the extremes of the desired tuning bandwidth. The smaller the ratio of the angles between 750 MHz and 1250 MHz, the greater the tuning range of the VCO. The results of the computer simulation are contained in the circuit file shown in Figure 12 and in Table 7.

A schematic diagram of the VCO using the AT-42086 buffer amplifier is shown in Figure 13. Actual measurements indicate that the computer simulation agrees well with bench measurements. The actual values of the interstage matching components vary only slightly from those calculated in the simulation program. The VCO tunes from 725 MHz to 1220 MHz with a tuning voltage from 1 to 20 volts and from 680 MHz to 1340 MHz with a 0 to 33 V tuning voltage. Power output over the 750 MHz to 1250 MHz range varies from +13 dBm to +16 dBm. Complete power output and second harmonic level versus frequency data is shown in Table 8.

Table 8. Performance of VCO using AT-41411 oscillator and AT-42086 buffer

Tuning Voltage V_t	Freq. MHz	Pwr Output dBm	2nd Harmonic Level -dBc
0	680	+15.0	-17
1	725	+15.6	-23
5	840	+15.8	-17
10	960	+16.2	-16
14	1000	+17.1	-
20	1220	+14.5	-
22	1255	+13.0	-
24	1280	+11.7	-
26	1300	+11.0	-
33	1340	+8.0	-

Conclusions

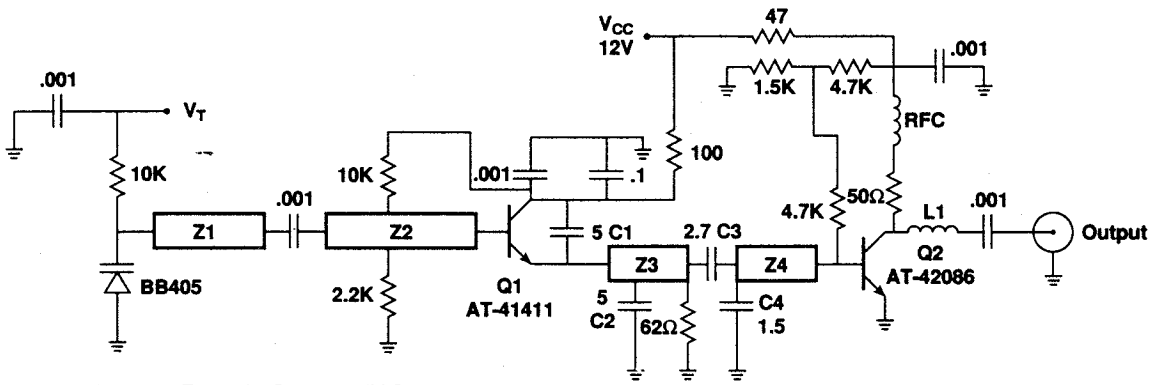
This note has described the design and performance of two L-band VCOs using an inexpensive silicon bipolar device as an oscillator and either a discrete or MMIC buffer amplifier stage. Several design concepts are covered along with several techniques that allow the use of linear analysis programs to design oscillators with performance comparable to the simulation. Although the linear analysis programs can not predict power output and spectral purity, they can predict frequency response and with reasonable accuracy determine circuit component values.

References

1. G. Vendelin, *Design of Amplifiers and Oscillators by the S Parameter Method*, John Wiley and Sons, Inc. 1982, pp. 139-145.

```
DIM
      FREQ GHZ
      IND NH
      CAP PF
      LNG IN
VAR
      !C1\2.01006

CKT
      MSUB    ER=4.8   H=.031   T=.0007   RHO=1   RGH=O

      S2PA    1    2    3       A:\S_DATA\BIP\AT41411G.S2P

      SLC     2    0            L=.5 C=1000

      MLIN    3    10           W=.10 L=.18
      SLC     10   0            L=.5 C=5
      MLIN    10   11           W=.10 L=.06
      SRL     11   0            R=62 L=.5
      SLC     11   12           L=.5   C\2.5
      MLIN    12   13           W=.10  L=.10

      MLIN    3    20           W=.10  L=.10
      SLC     20   21           L=.5 C=4.7
      MLIN    21   2            W=.02  L=.07

      MLIN    13   30           W=.05  L=.25
      MLIN    30   31           W=.07  L=.25
      SLC     30   0            L=.5 C\1.9

      S2PB    31   32   33      A:\S_DATA\BIP\AT42086G.S2P
      MLIN    33   34           W=.020 L=.020
      MLIN    33   35           W=.020 L=.020
      VIA     34   0            D1=.025 D2=.025   H=.031   T=.0007
      VIA     35   0            D1=.025 D2=.025   H=.031   T=.0007

      MLIN    32   36           W=.O9 L=.O9
      IND     36   37           L=6
      SLC     37   38           L=.5 C=10
      MLIN    38   39           W=.08 L=.18

      SRL     36   40           R=100 L=.5
      IND     40   41           L=100
      SLC     41   0            L=.5 C=1000

      DEF2P   1    39           OSC
```

Figure 12. AT-41411/AT-42086 VCO Circuit



L1 1 Turn #24 Gauge 0.1" I.D.
RFC .1 uH Miniature RF Choke

Z1-Z4 Etched Microstrip Circuitry

Figure 13. Schematic Diagram VCO with Transistor Buffer