M3300A-01

Modification Recommended Service Note

Supersedes:
[NONE]

M3300A PXIe AWG and Digitizer Combination

Serial Numbers: MY57080100 - MY57479999
ES56600101 - ES56600145

The Problem – D.C offset error on the AWG output due to:

1. A possible short circuit between the SMT ceramic output filter terminal and PCB ground plane.
2. A manufacturing change in ceramic filter performance that lead to unstable DC offset performance.

Parts Required:
NONE - Return to Factory

ADMINISTRATIVE INFORMATION

ACTION CATEGORY:	[ ] ON SPECIFIED FAILURE [X] AGREEABLE TIME	STANDARDS LABOR: 1.0 Hours			
LOCATION CATEGORY:	[ ] CUSTOMER INSTALLABLE [ ] ON-SITE (active On-site contract required) [X] SERVICE CENTER [ ] CHANNEL PARTNERS	SERVICE INVENTORY:	[X] RETURN [ ] SCRAP [ ] SEE TEXT	USED PARTS:	[X] RETURN [ ] SCRAP [ ] SEE TEXT
AVAILABILITY: PRODUCT'S SUPPORT LIFE		NO CHARGE AVAILABLE UNTIL: Feb 1st 2019			
[X] Calibration Required [ ] Calibration NOT Required		PRODUCT LINE: PLBL AUTHOR: [PR]			

ADDITIONAL INFORMATION: Return to Factory repair and calibration

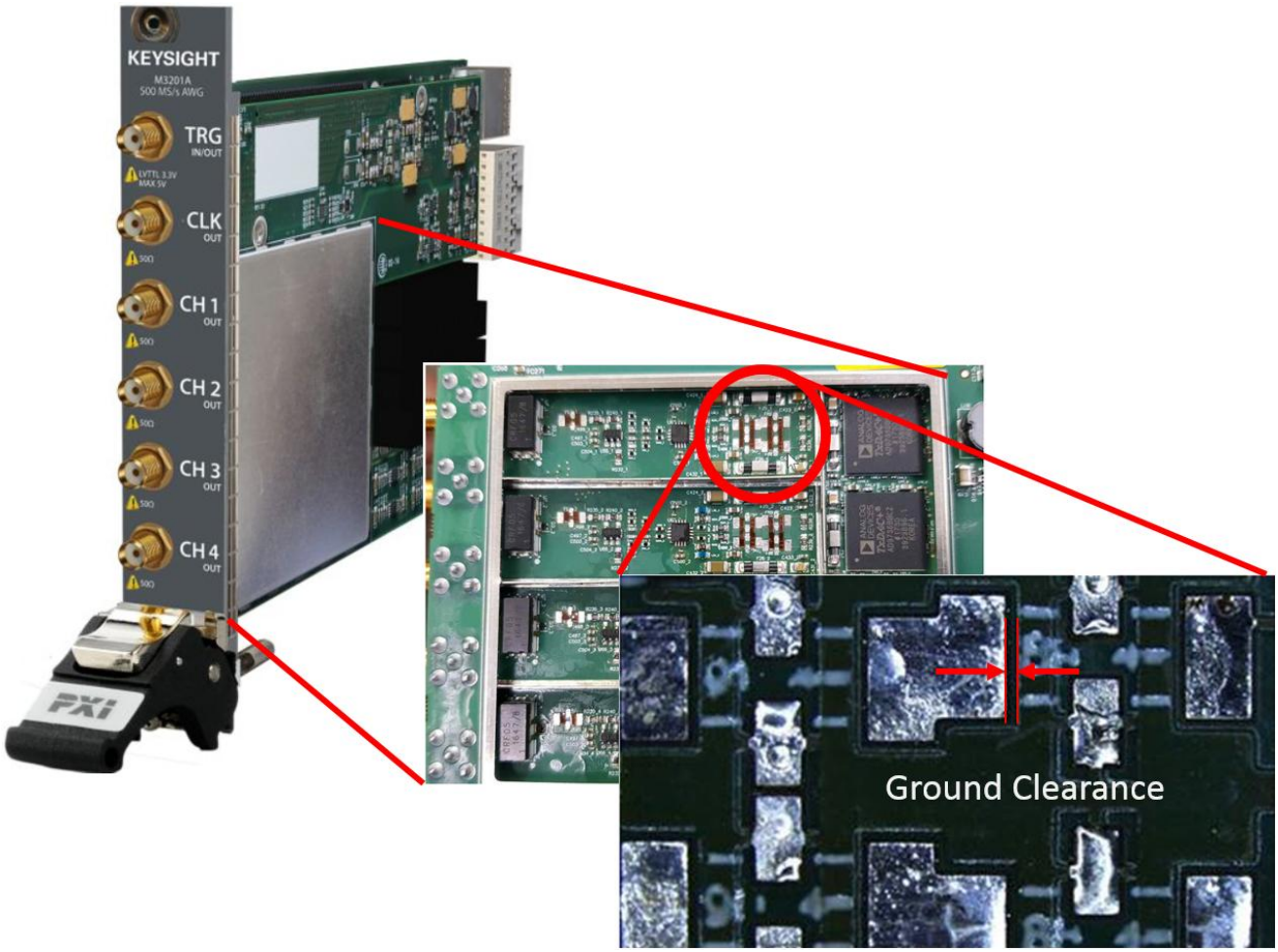
KEYSIGHT TECHNOLOGIES

Situation:
A ceramic filter developed by Minicircuits is used in the AWG source output path to minimize source harmonics and spurs. The PXIe Arbitrary Waveform Generators: M3201A & M3202A and PXIe AWG and Digitizer Combo cards M3300A & M3302A can suffer a D.C offset error in the output signal due to a combination of two factors attributed to this filter:

1. A possible short circuit between the filter output pad and the PCB ground plane due to insufficient ground clearance in the PCB design.

1. The performance of the filter changed sometime in 2017 which was not picked up by Keysight. This resulted in unstable DC offset performance after being in operation for some time.

The ground plane clearance problem can be seen below:

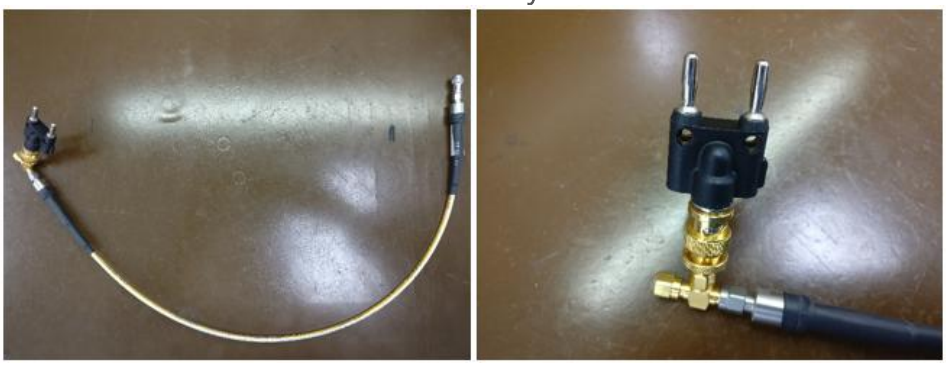


These problems have been fixed in all modules, M3201A & M3202A, M3300A & M3302A from MY57510001 onwards.

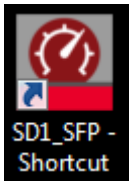
Solution/Action:
The problem can show up as either a constant or intermittent DC offset issue which is significantly larger than the specified DC offset characteristics of the module

The DC offset is easily measured using a DVM, SMA test cable, banana jack, T splitter and 50Ω load. If you do not have a 50Ω load check the HiZ output in the instructions below.

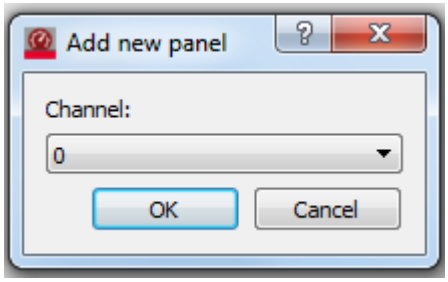
Procedure to check the DC offset accuracy



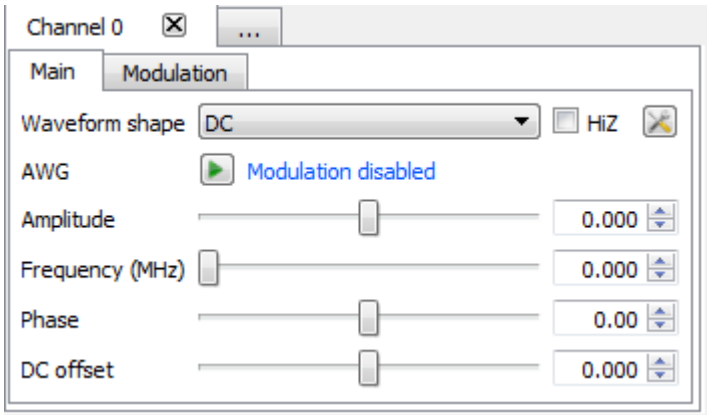
1. Start Keysight SD1 Soft Front Panel software



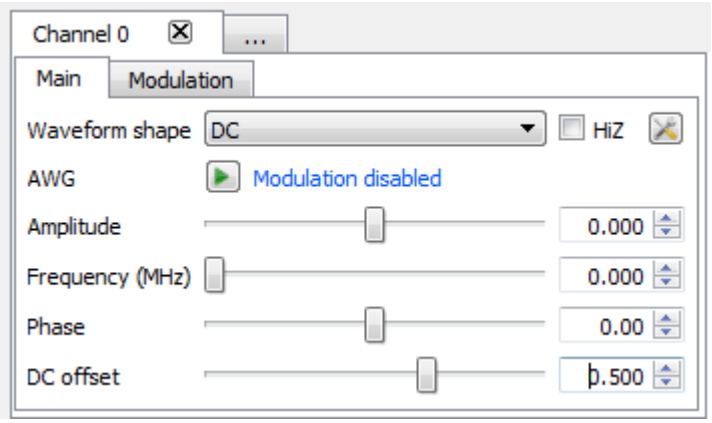
2. Add panels 1, 2, 3, 4 by clicking View | New Panel ...



3. 0V Offset – Change Waveform shape to “DC”, untick HiZ, measure channel output (if using the 50Ω load) with a DMM and record this.



4. 0.5V Offset – With the same settings, change DC offset to 0.5 V.



5. Repeat 0V Offset and 0.5V Offset test for each channel.
6. Average about 3 to 4 measurements to filter out random noise
7. Tabulate the results and compare vs the limits.

	CH1 (average)	CH2 (average)	CH3 (average)	CH4 (average)	LL (Vdc)	UL (Vdc)
0V Offset					-0.1	+0.1
0.5V Offset					0.4	0.6

PXIe AWG M3201A & M3202A and PXIe AWG and Digitizer Combo M3300A & M3302A exhibiting excessive DC offset can be returned to keysight for repair and full calibration.

Revision History:

Date	Service Note Revision	Author	Reason for Change
08 Feb 2018	01	Paul Rooney	As Published