

M8062A-03

# Modification Recommended Service Note

Supersedes:  
NONE

## M8062A - 32 Gb/s Front-End for J-BERT M8020A High-Performance BERT

Serial Numbers: MY55120057, MY55120063, MY55120068, MY55120073, MY55400301, MY55400302, MY55400303, MY55400304, MY55400305, MY55400306, MY55400307, MY55400311, MY55400312, MY55400315, MY55400316, MY55400317, MY55400318, MY55400319, MY55400321, MY55400323, MY55400324, MY55400326, MY55400327, MY55400328, MY55400329, MY55400330

**The Problem:** When using the CDR as the M8062A Analyzer Clock Source and operating at data rates near 8 Gbps (4 GHz clock frequency), some units may experience elevated jitter levels on the recovered clock, as measured at the Analyzer Clock Out connector.

Parts Required: NONE

### ADMINISTRATIVE INFORMATION

ACTION	<input type="checkbox"/> ON SPECIFIED FAILURE	STANDARDS			
CATEGORY:	X AGREEABLE TIME	LABOR:	1.0 Hours		
LOCATION	<input type="checkbox"/> CUSTOMER INSTALLABLE	SERVICE:	X RETURN	USED	X RETURN
CATEGORY:	<input type="checkbox"/> ON-SITE (active On-site contract required)	INVENTORY:	<input type="checkbox"/> SCRAP	PARTS:	<input type="checkbox"/> SCRAP
	X FACTORY		<input type="checkbox"/> SEE TEXT		<input type="checkbox"/> SEE TEXT
	<input type="checkbox"/> CHANNEL PARTNERS				
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	NO CHARGE AVAILABLE UNTIL:	PRODUCT'S SUPPORT LIFE		
	X Calibration Required	PRODUCT LINE:	PL24		
	<input type="checkbox"/> Calibration NOT Required	AUTHOR:	MM		

### ADDITIONAL INFORMATION:

Hardware modification can be performed at the Factory only.

**Situation:**

When the CDR is selected as the M8062A analyzer clock source (Data In > Clock > Source) and the system is operating at data rates around 8 Gbps (4 GHz clock frequency) the recovered clock from the CDR may have excessive noise, observable as elevated jitter levels on the analyzer clock output.

- The affected data rate range is typically between 8.0 – 8.25 Gbps (4.0 – 4.125 GHz clock).
- Units without this problem typically have 0.5 ps or less of  $RJ_{RMS}$  on the analyzer clock output.
- Units with this problem typically have 1 ps or more of  $RJ_{RMS}$  on the analyzer clock output.
- This problem may be intermittent – the frequency and amplitude of the noise can change.

There is no expected impact to performance when:

- Operating at other data rates.
- “SYS CLK” or “CLK IN” is selected as the analyzer clock source.

**Solution/Action:**

A board level hardware modification (M8062-66804 Mod 7) exists which fixes this problem. This modification is to be performed at the Factory only.

This modification is to be performed on all listed units sent to the Factory for calibration or repair, even if the failure symptom is not observable. Implementation of this modification is to be performed at the expense of the Factory. The customer may be charged for failures found on incoming test which are not related to this modification.

It is necessary to run full performance verification after this modification has been performed.

**Revision History:**

Date	Service Note Revision	Author	Reason for Change
12 April 2016	01	MM	As Published