S E R V I C E N O T E

SUPERSEDES: NONE

Z5210F INS DDC Module

Serial Numbers: 0000A00000 / 9999Z99999

To Be Performed By: Agilent-Qualified Personnel

Parts Required:

P/N	Description	Quantity
Z5210-80003	DSP EPROM	1
Z5210-80004	EPLD EPROM	1

Situation:

Update to the latest firmwares to address the following problems.

DDC DSP

Firmware Rev.	Problems Addressed
Version 1.1	Initial version for -135 dBc/Hz @ 500kHz Offset DDC. Changes made to accommodate new modulator.
Version 1.2	1) Ring Channel not transmitting with 9 msec propagation delay. 2) Transmit timing off by as much as 1 ?s.
Version 1.3	1) Maximum dynamic range of DDC card was wrong.
Version 1.4	1) Traffic Channel transmitting incorrect data when propagation delay is 8.28 msec.
Version 1.5	1) Intermittent continuous wave mode.

Continued

DATE: December 1998

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

MODIFICATION RECOMMENDED

ACTION CATEGORY:	☐ IMMEDIATELY ☐ ON SPECIFIED FAILURE ■ AGREEABLE TIME	STANDARDS: LABOR 0.5 Hours			
LOCATION CATEGORY:	☐ CUSTOMER INSTALLABLE ■ ON-SITE ■ SERVICE CENTER	SERVICE INVENTORY:	☐ RETURN ☐ SCRAP ☐ SEE TEXT	USED PARTS:	☐ RETURN ■ SCRAP ☐ SEE TEXT
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	AGILENT RESPONSIBLE UNTIL: December 1999			
AUTHOR: BJ	ENTITY: 4222	ADDITIONAL INFORMATION:			

Agilent Technologies

DDC DSP

Firmware Rev.	**Problems Addressed**
Version 1.6	1) Changed the semaphore handshake to allow for a slow host. 2) Added extended information to the error code primitives for frame number and time fields.
Version 1.7	1) Removed the assertion of the SYSFAIL signal upon receiving a software error (i.e., DDC 0x0804 missed deadline time). This can (in conjunction with another VME IRQ) cause the Pentium controller to lockup.
Version 1.8	1) Fixed a problem in the "send_tch_voice" primitive for fax/data.

DDC EPLD

Firmware Rev.	**Problems Addressed**
Version 1.0	Original Motorola version of the EPLD code.
Version 1.1	1) Fixed many clocking problems in the original code. Basic functionally stayed the same.
Version 1.2	1) Fixed a problem that occurred when using the DDC in a MXI controlled card cage.
Version 1.3	1) Removed the use of the 16 MHz clock in the EPLD. This clock was bleeding through causing spurs in the output
Version 1.4	1) Fixed a problem with the DDC card intermittently missing the start of test pulse.

Solution / Action:

Replace the previous version with the latest version:
Z5210F-80003 Rev. 1.8 and Z5210-80004 Rev. 1.4
Upgrade DDC Firmwares Instruction

1. De-power the system and take out Z5210F DDC cards.

2. Based on the board facing vertically, remove the side cover by taking out the 3 screws on the front right side, 6 screws from the top and bottom, and 1 screw in the back. All together total of 16 screws.

3. Replace the existing EPROM Z5210-80003 (DSP) with provided Z5210-80003 Rev 1.8 at ref. designate U204. When replace, EPROM notch must faces towards the white dot (represents pin 1) that was mask on the PC board.

4. Replace the existing EPROM Z5210-80004 (EPLD) with provided Z5210-80004 Rev 1.4 at ref. designate U611. When replace, EPROM notch must faces towards the white dot (represents pin 1) that was mask on the PC board.

5. Install the side cover back with the 16 screws that were removed.

6. Affix label to front panel just above the serial number label with the provided label (DSP Rev 1.8, EPLD Rev 1.4).

7. Reinstall the DDC cards to the same slot locations.

8. Power up the system.

9. Run the "Ready Check" test in the SFT menu 1 to verify that the DDC cards are good.